

FIG. 2

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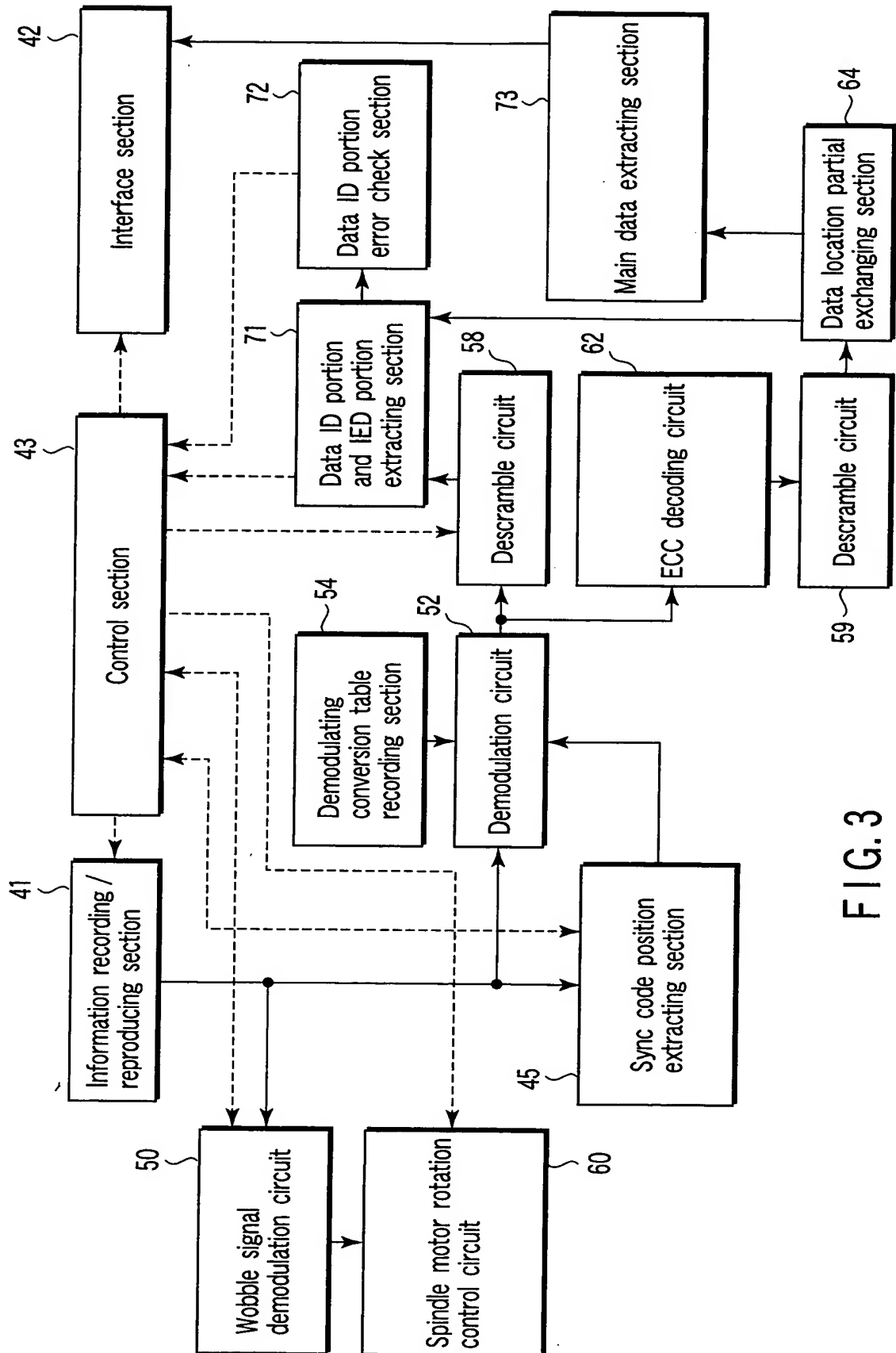


FIG. 3

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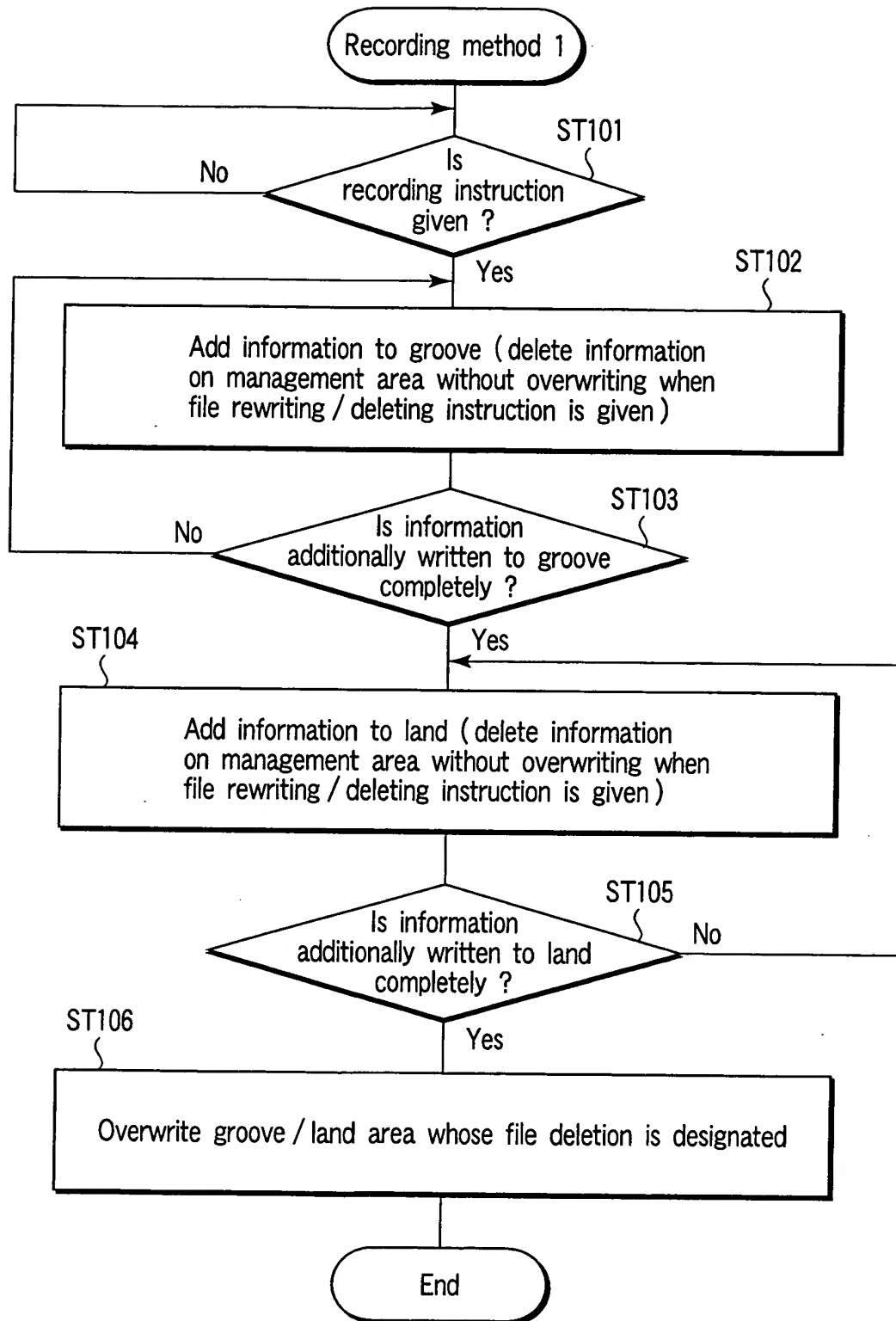


FIG. 4

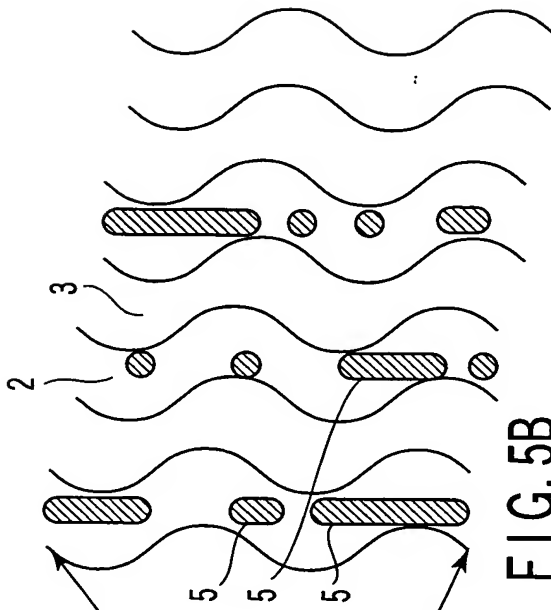


FIG. 5A

FIG. 5B

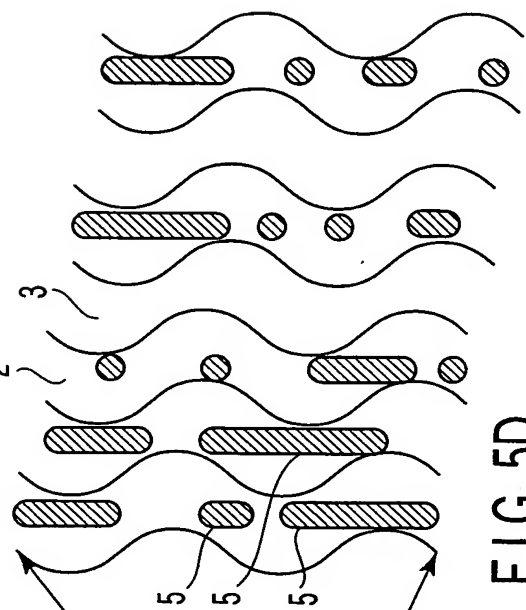
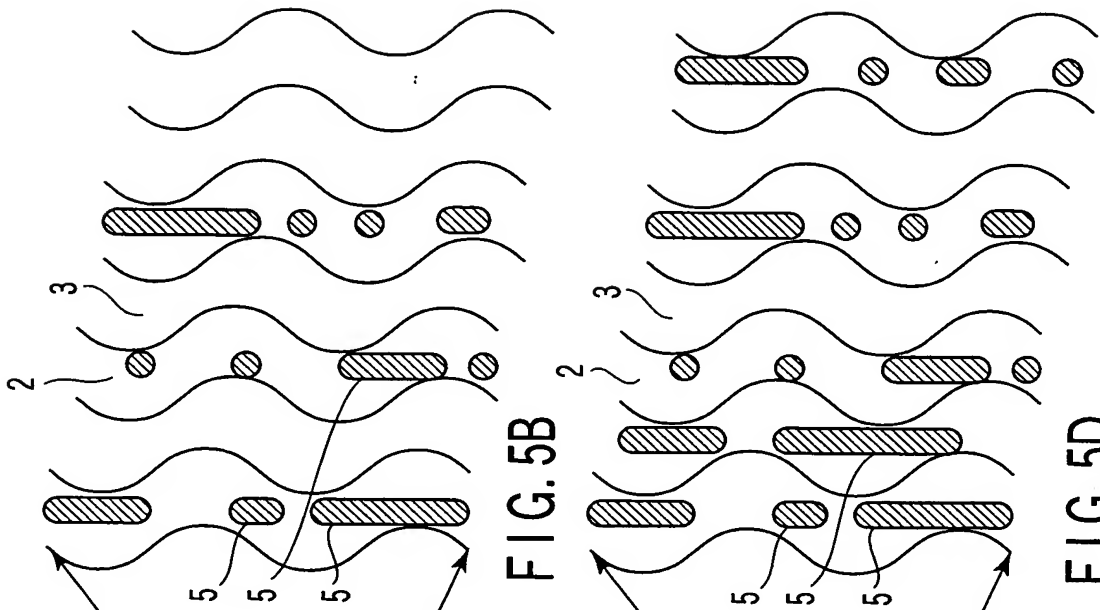


FIG. 5C

FIG. 5D



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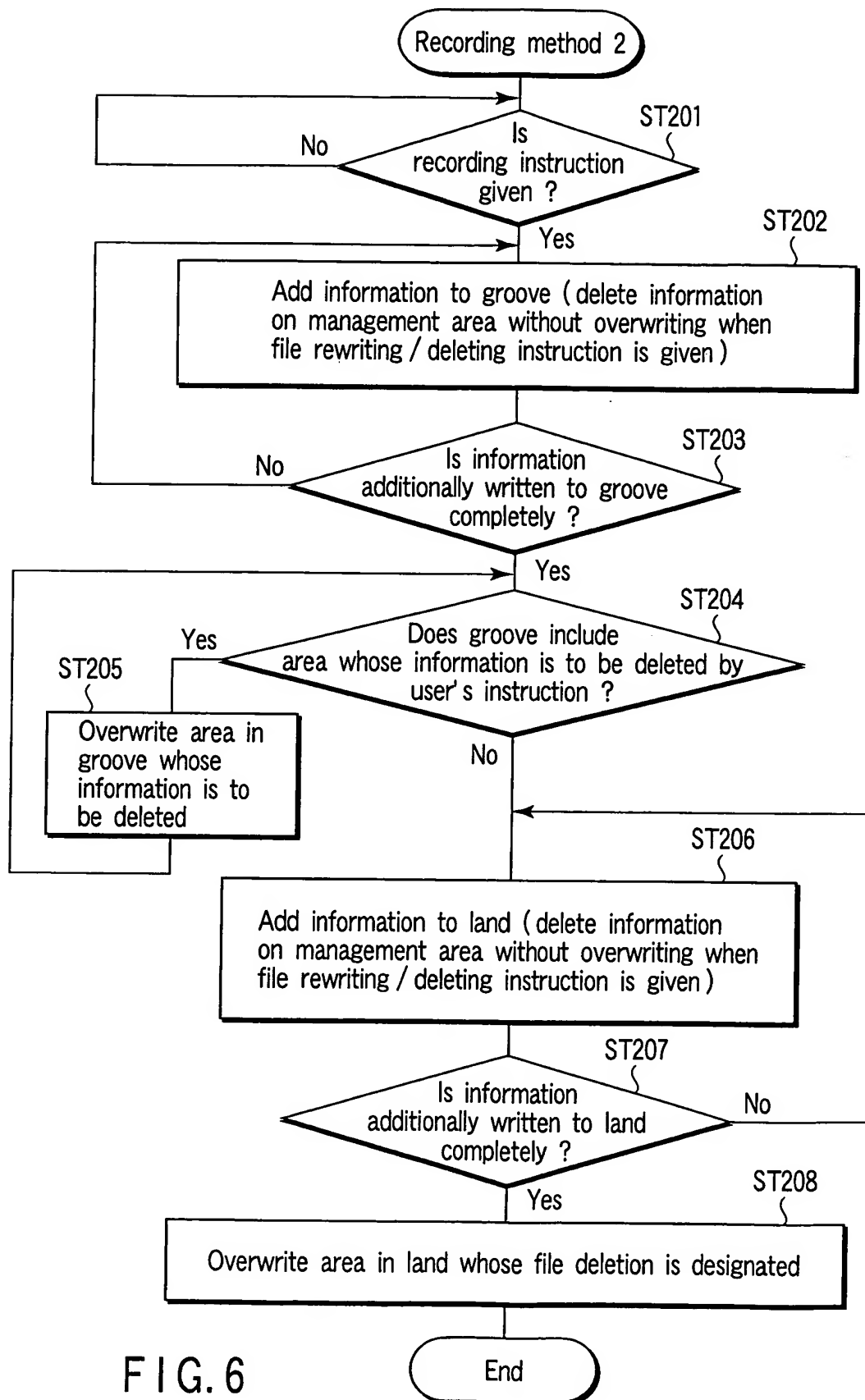


FIG. 6

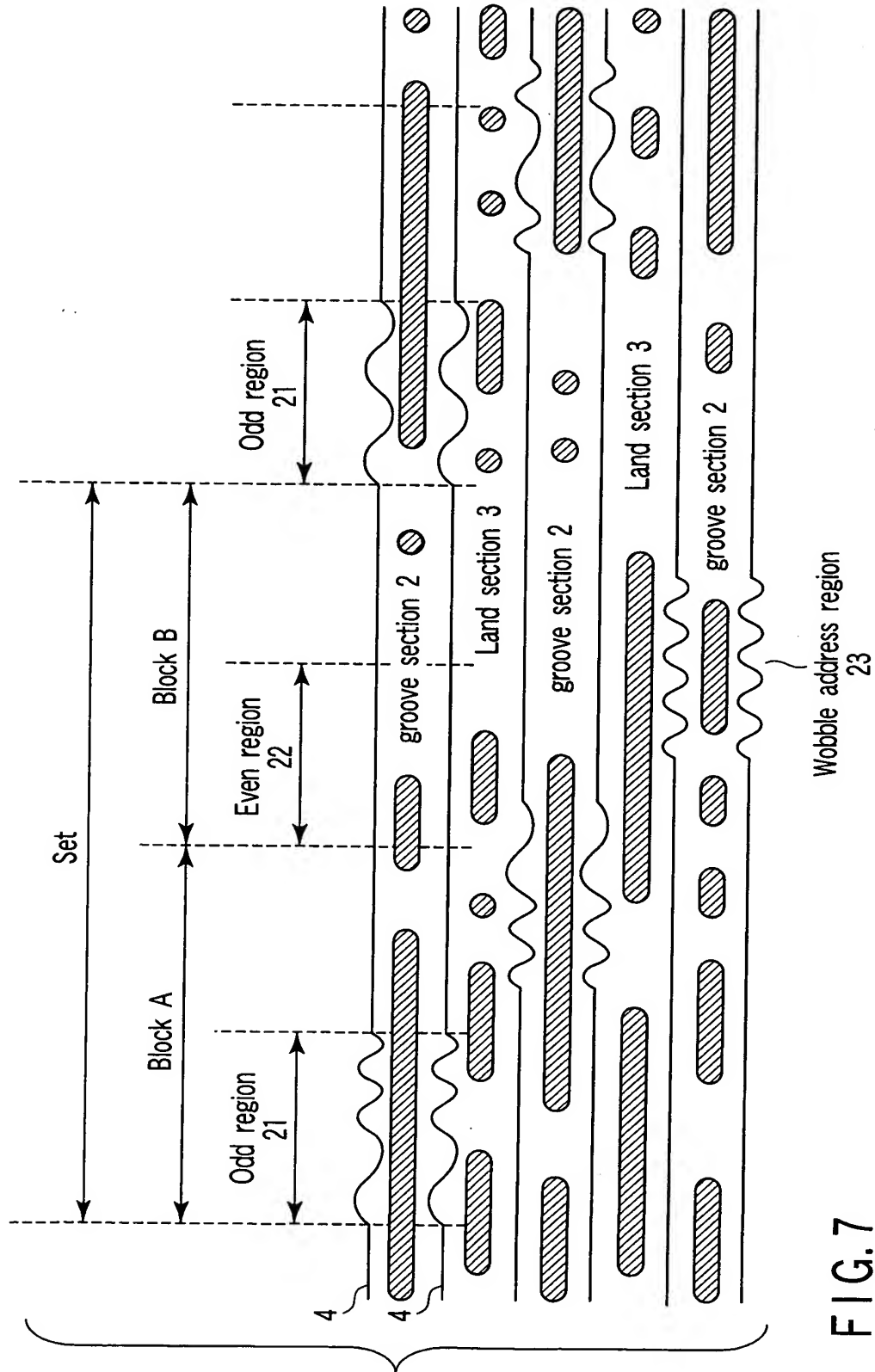
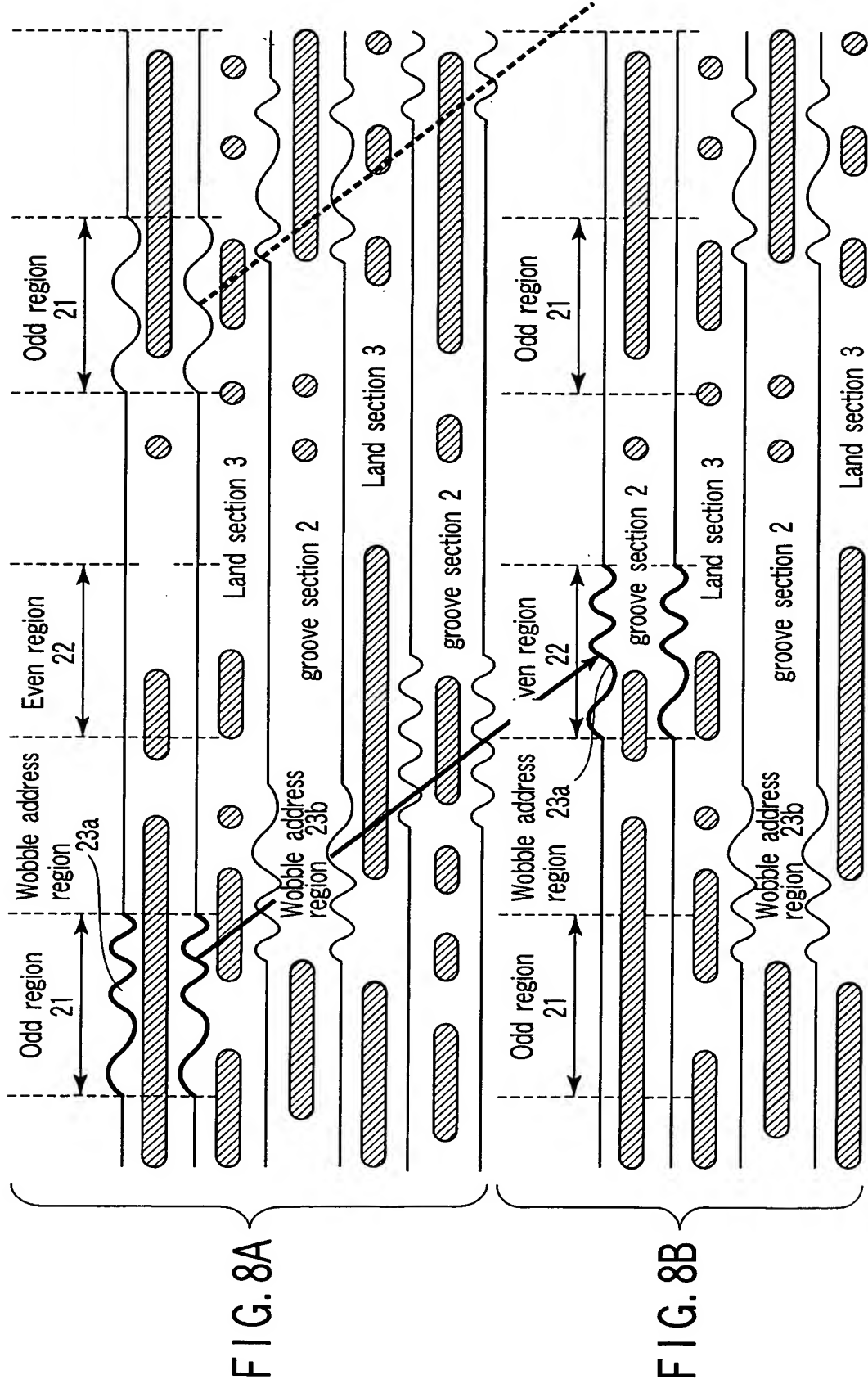


FIG. 7



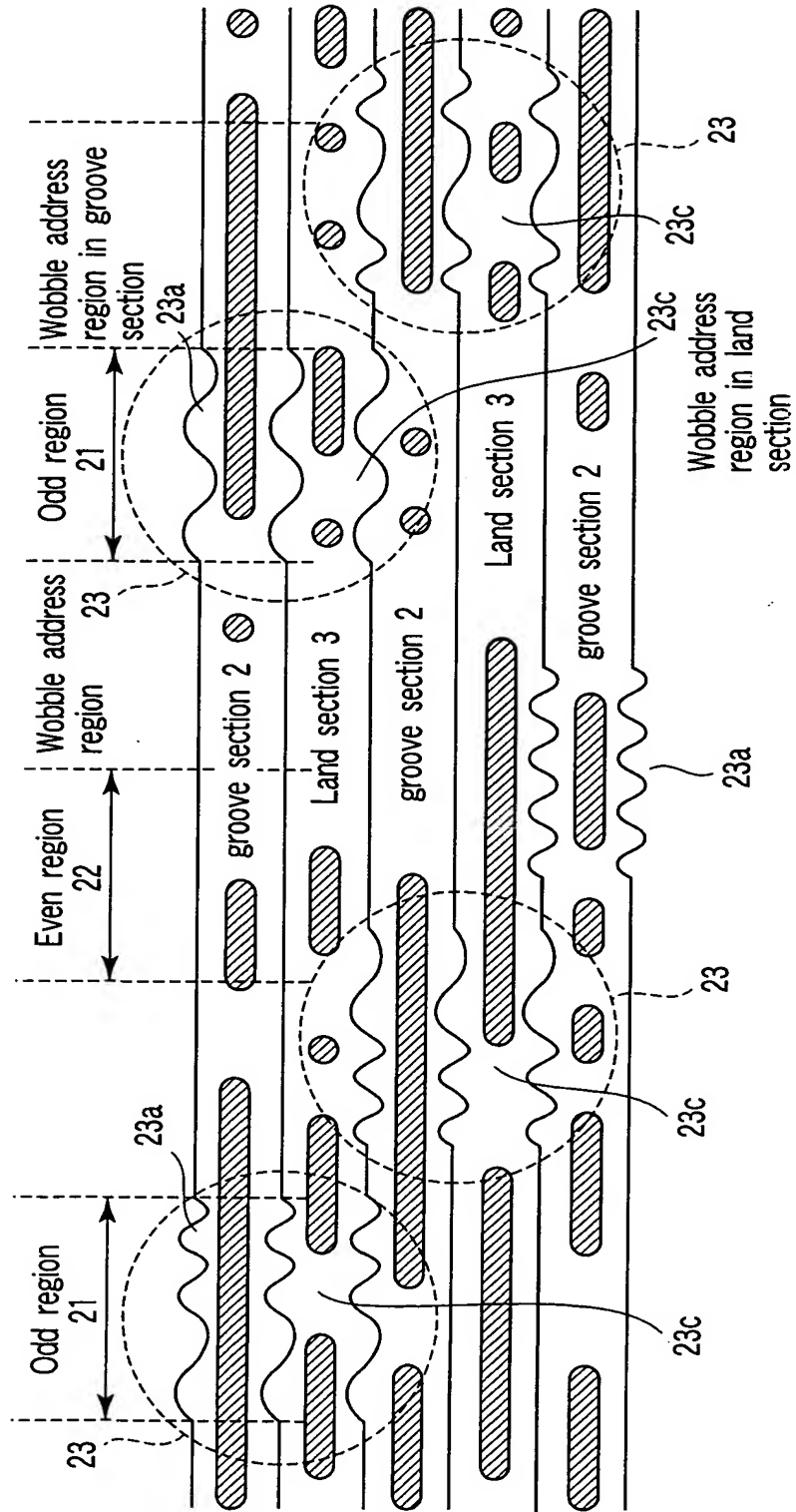


FIG. 9

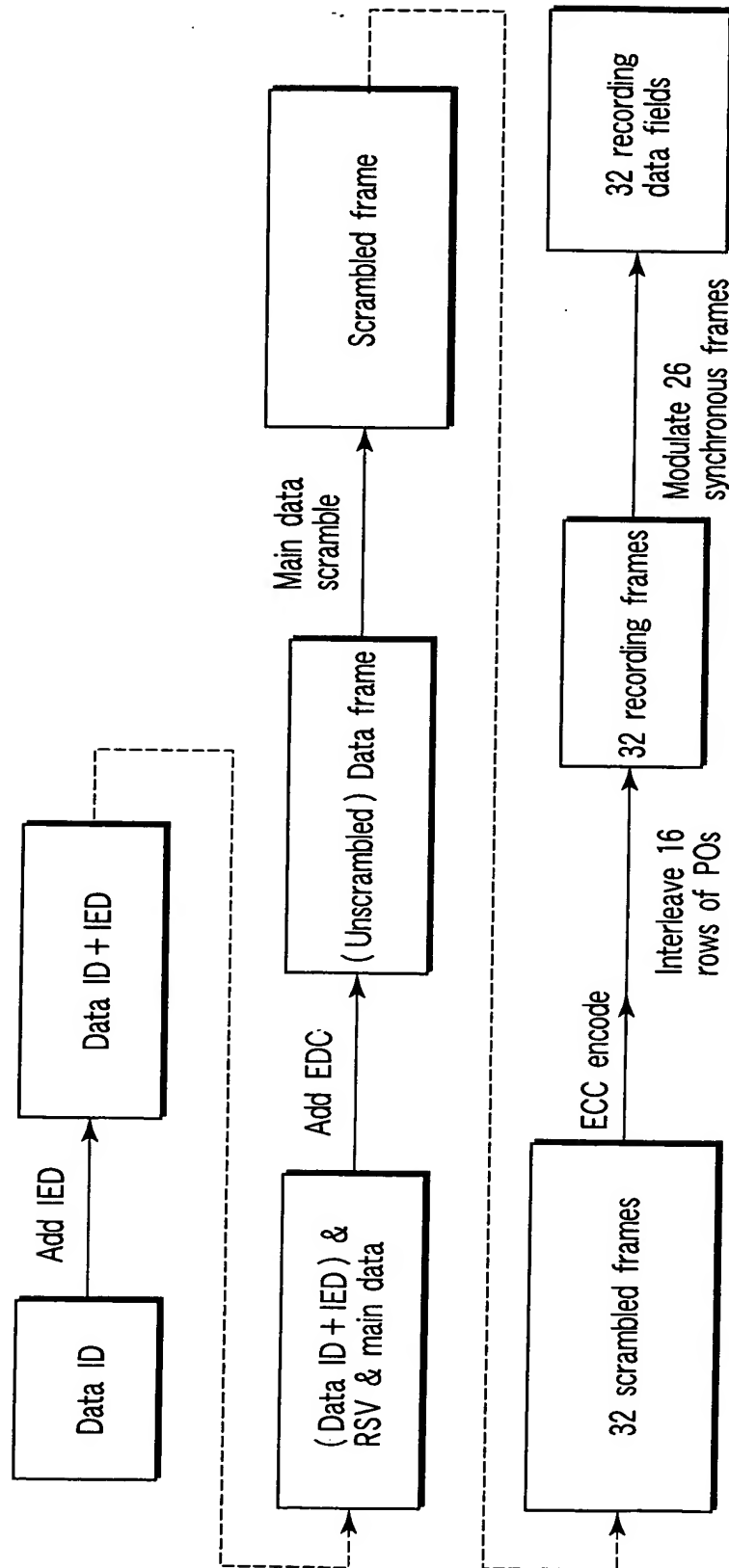


FIG.10

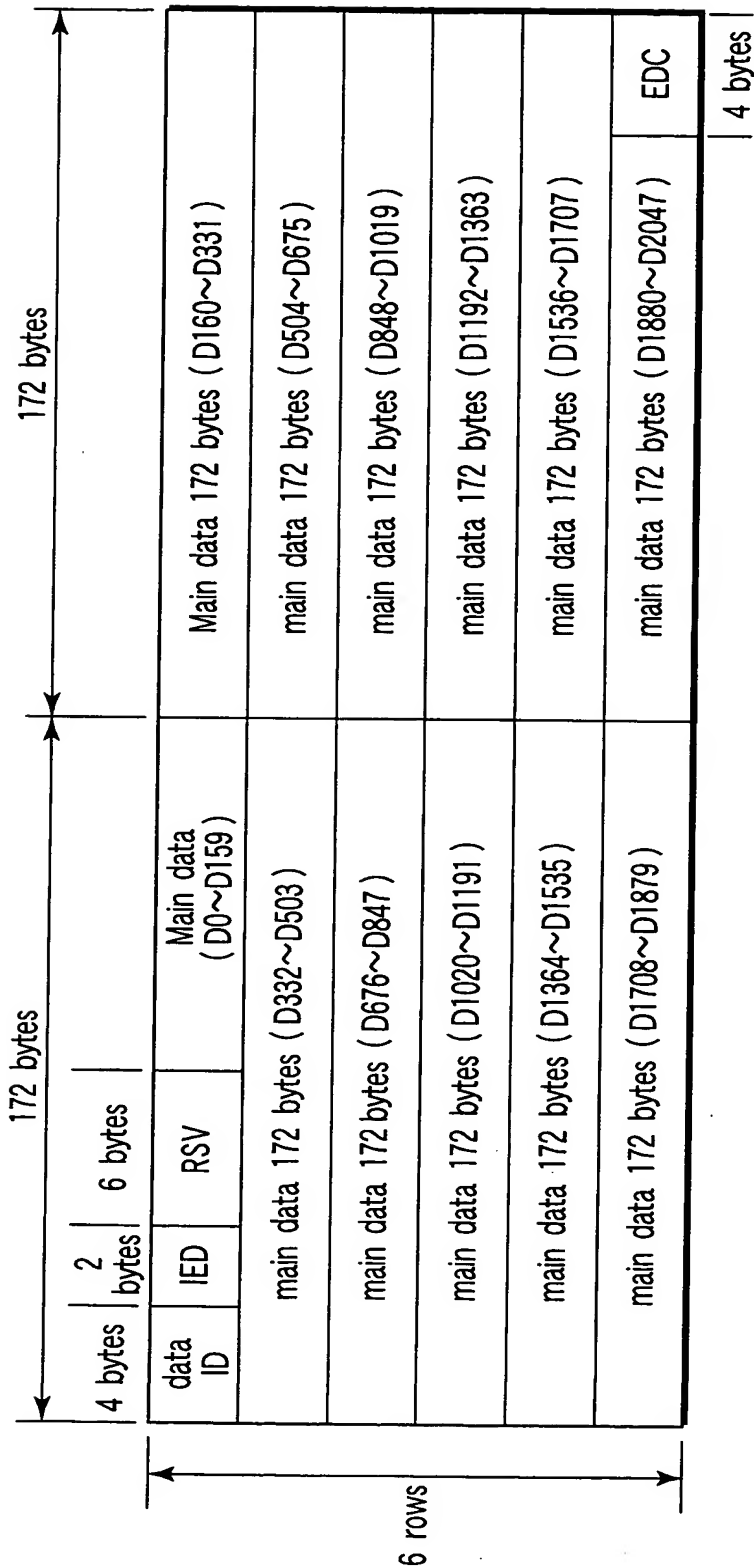


FIG.11

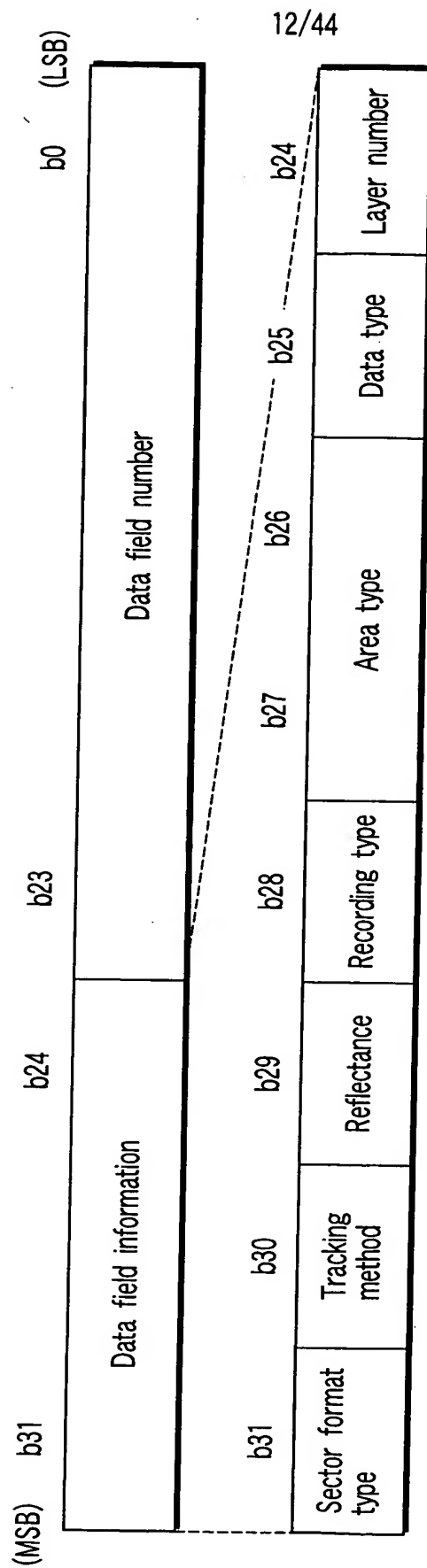


FIG. 12

Area	Contents
Embossed data zone	Sector number
Defect management area	Sector number
Disk identification zone	Sector number
Block used in data area	LSN + 031000h
Block unused in data area	One of state 1 : first 3 bits are 0 and number is subsequently incremented, state 2 : between 00 0000h and 00 00Hh, and state 3 : Unrecorded

FIG. 13

Area		Contents
Embossed data zone		Reserved
Rewritable data zone	Lead-in area, lead-out area	Reserved
	Data area	0b : General data 1b : Real-time data

FIG. 14

Initial preset number	Initial preset value	Initial preset number	Initial preset value
0h	0001h	8h	0010h
1h	5500h	9h	5000h
2h	0002h	0Ah	0020h
3h	2A00h	0Bh	2001h
4h	0004h	0Ch	0040h
5h	5400h	0Dh	4002h
6h	0008h	0Eh	0080h
7h	2800h	0Fh	0005h

Initial value in shift register

FIG. 15A

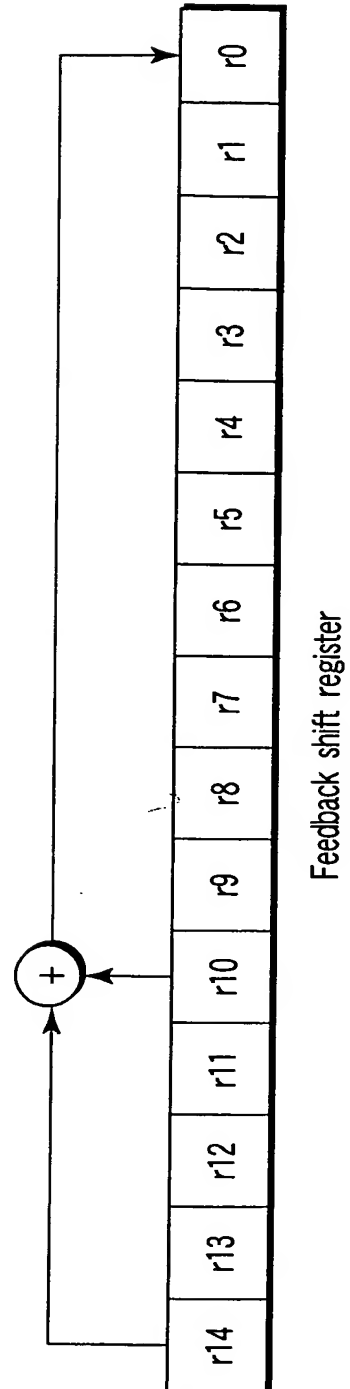


FIG. 15B



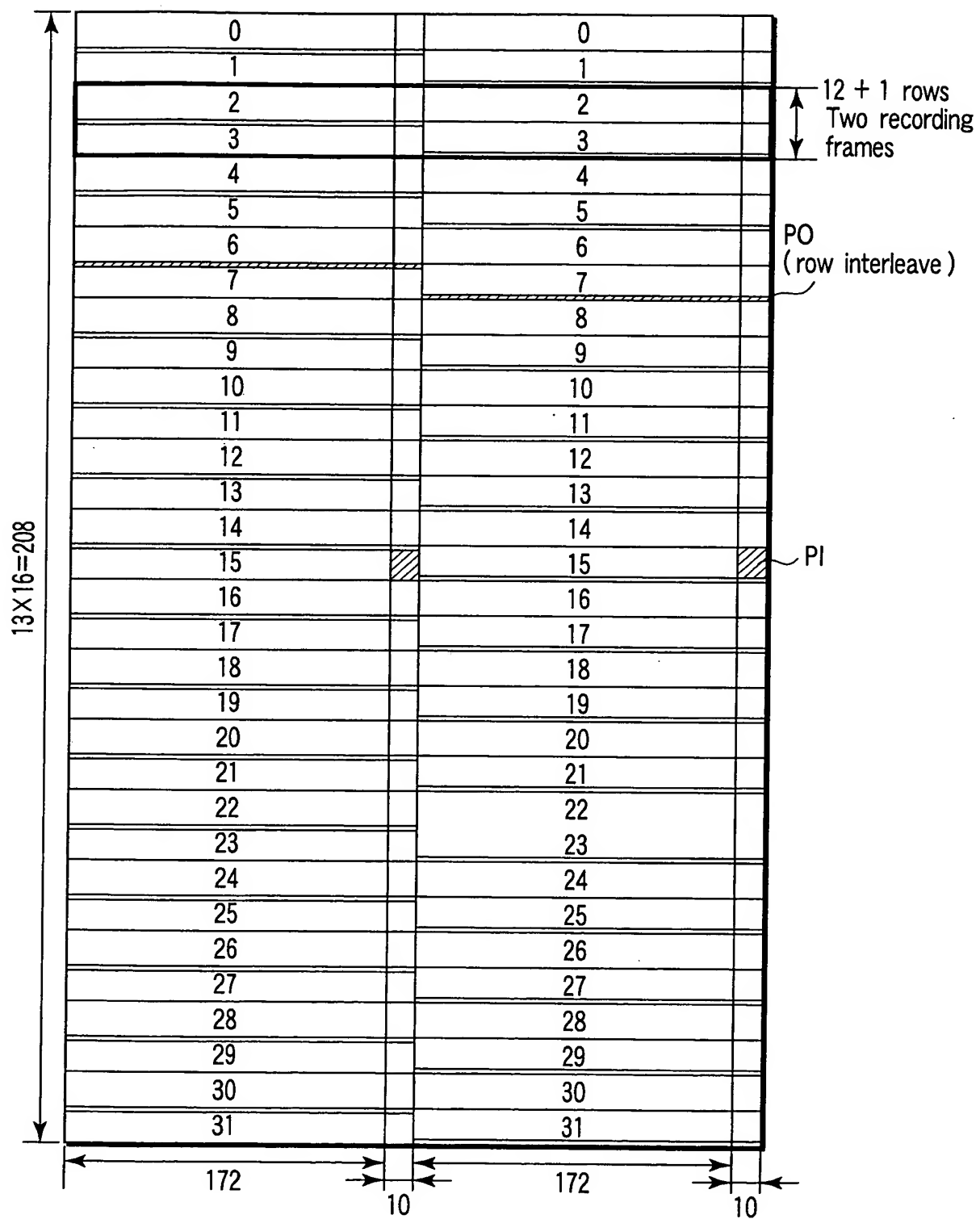


FIG. 18

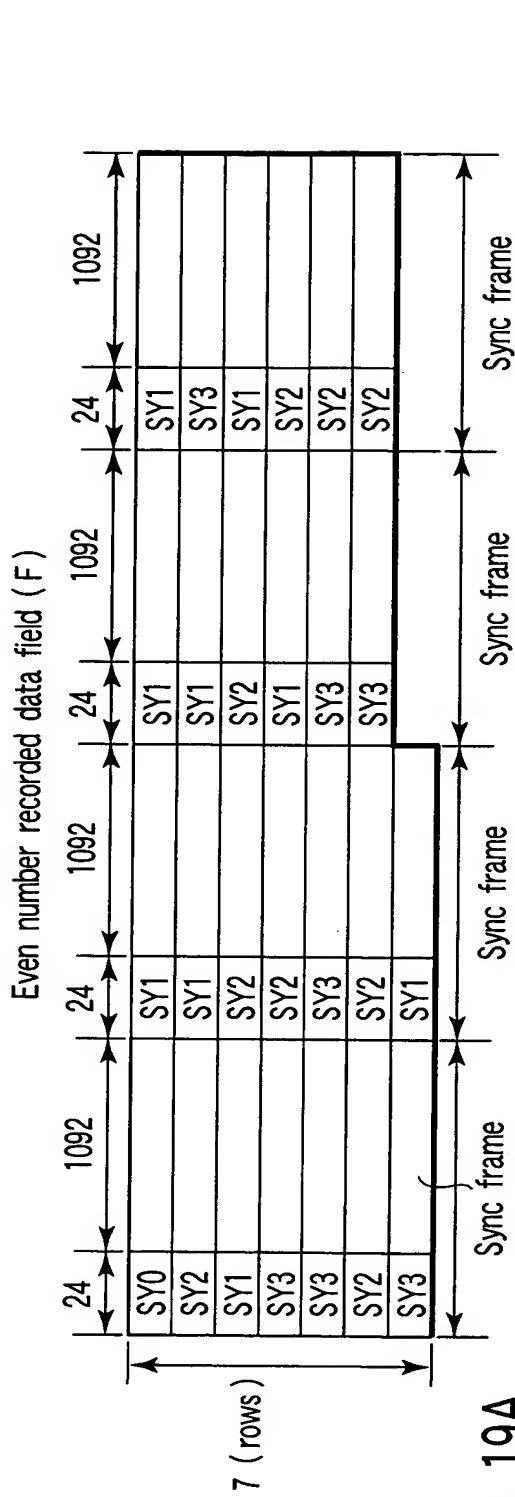


FIG. 19A

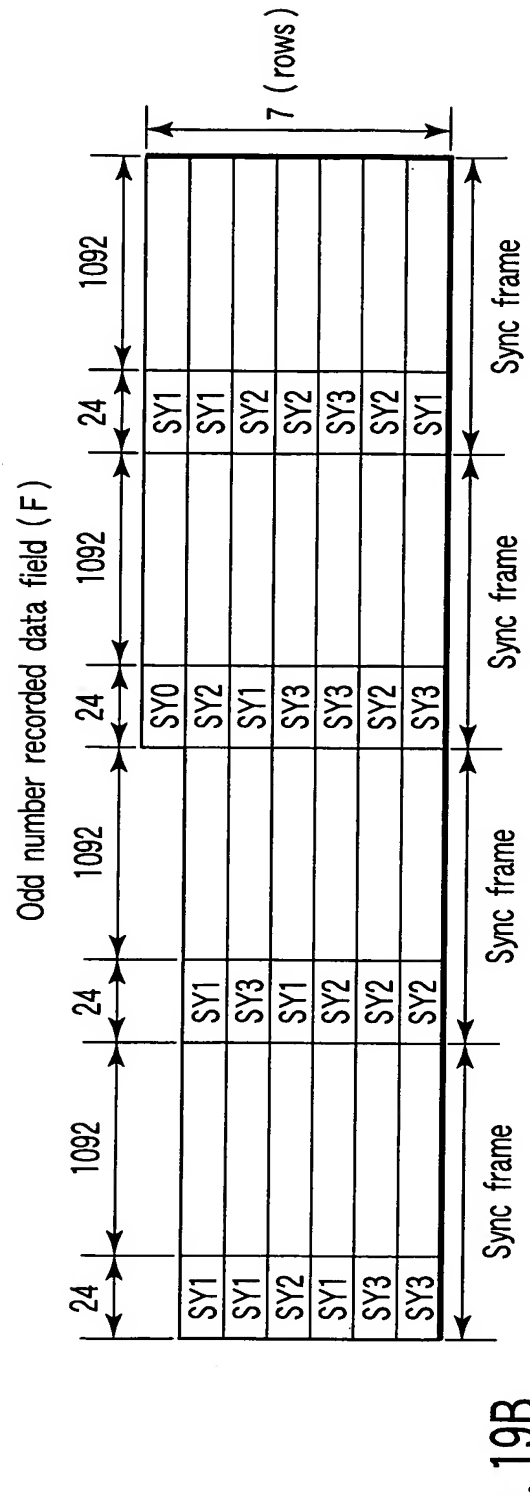


FIG. 19B

<u>State 0</u>		(MSB) First SYNC code (LSB)		(MSB) Second SYNC code (LSB)	
SY0	=	000010	101000	000000	001001 / 000010 001000 000000 001001
SY1	=	100001	001000	000000	001001 / 100010 101000 000000 001001
SY2	=	100100	001000	000000	001001 / 101000 101000 000000 001001
SY3	=	101000	001000	000000	001001 / 101010 001000 000000 001001
<u>State 1</u>		(MSB) First SYNC code (LSB)		(MSB) Second SYNC code (LSB)	
SY0	=	000100	101000	000000	001001 / 000100 001000 000000 001001
SY1	=	001001	001000	000000	001001 / 001010 101000 000000 001001
SY2	=	010000	101000	000000	001001 / 010000 001000 000000 001001
SY3	=	010100	001000	000000	001001 / 010101 001000 000000 001001

Sync code

FIG. 20

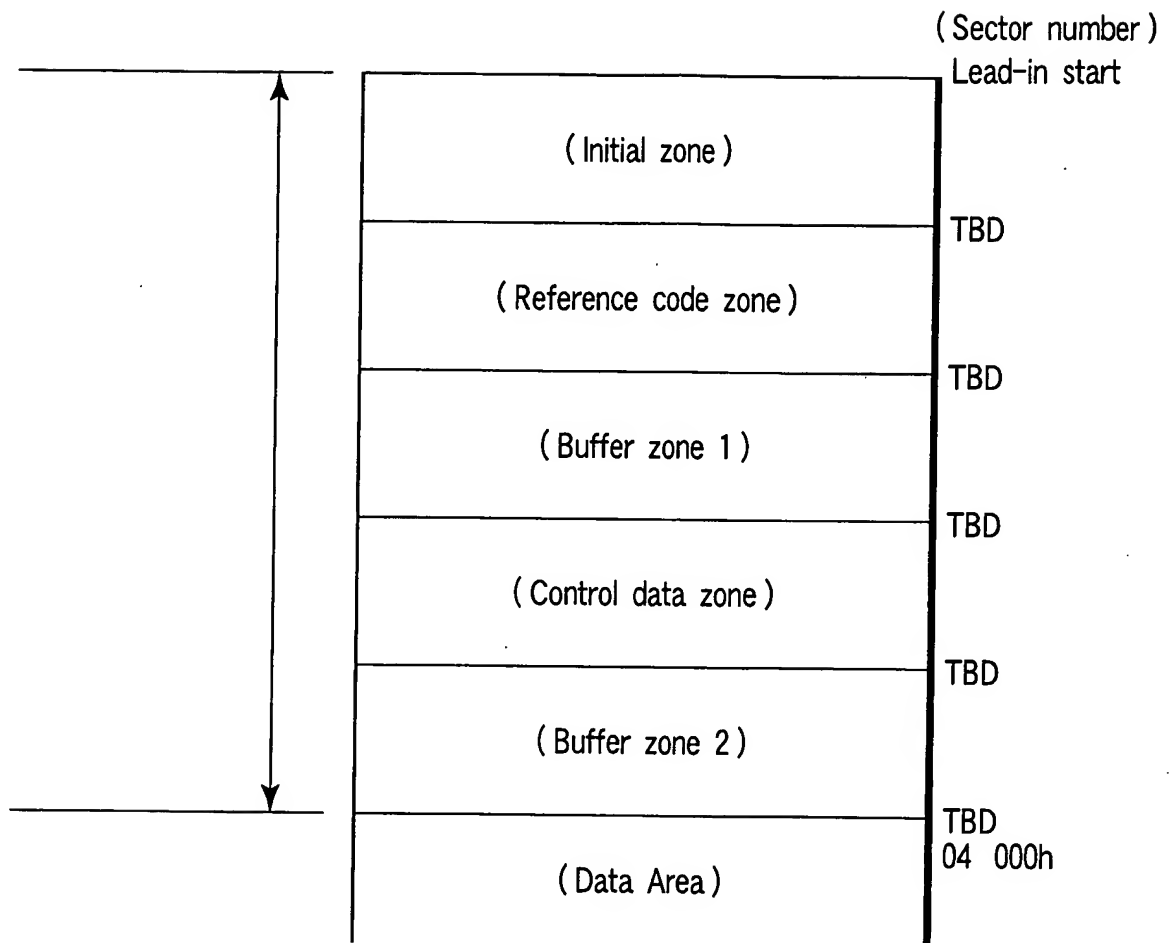


FIG. 21

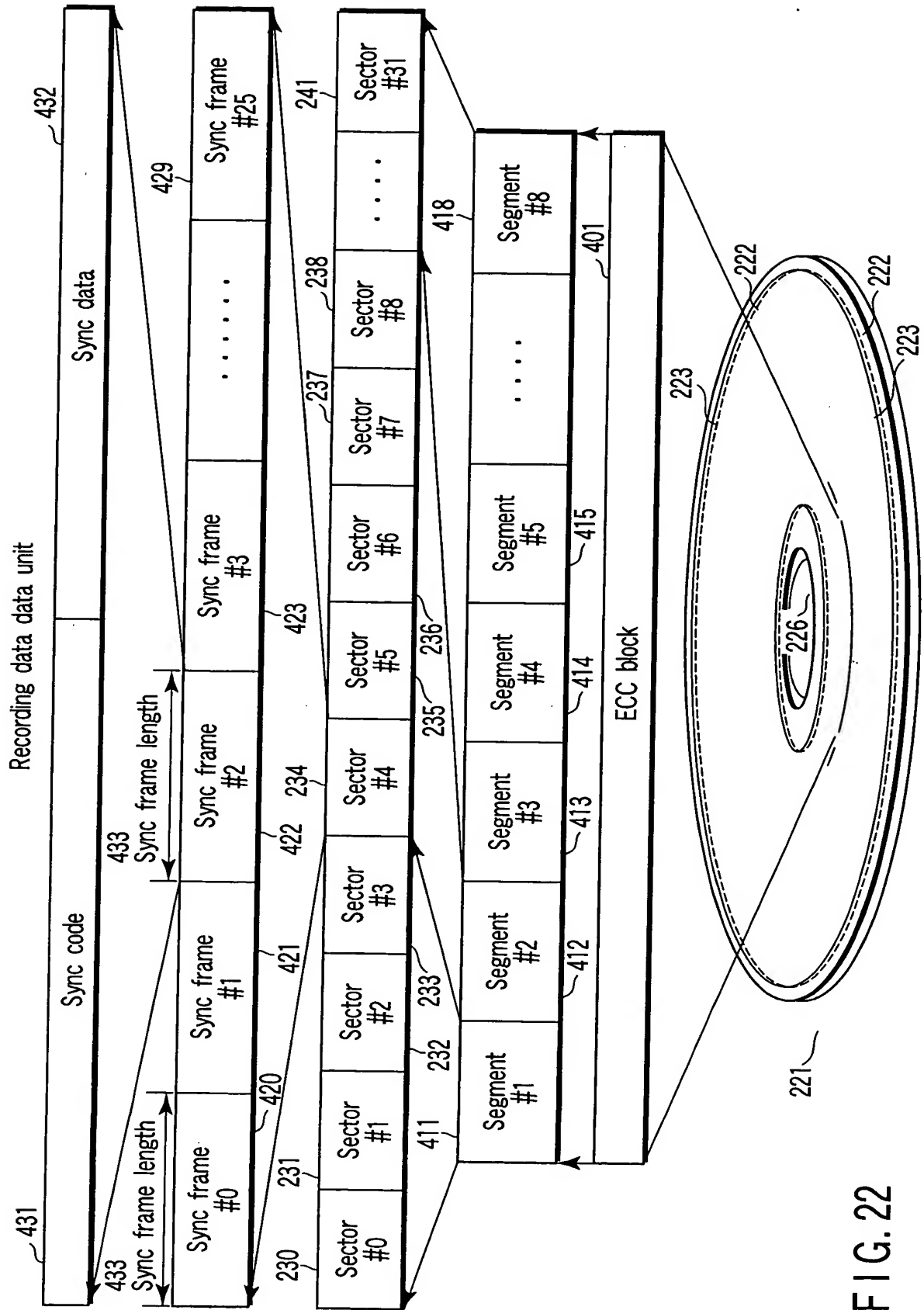
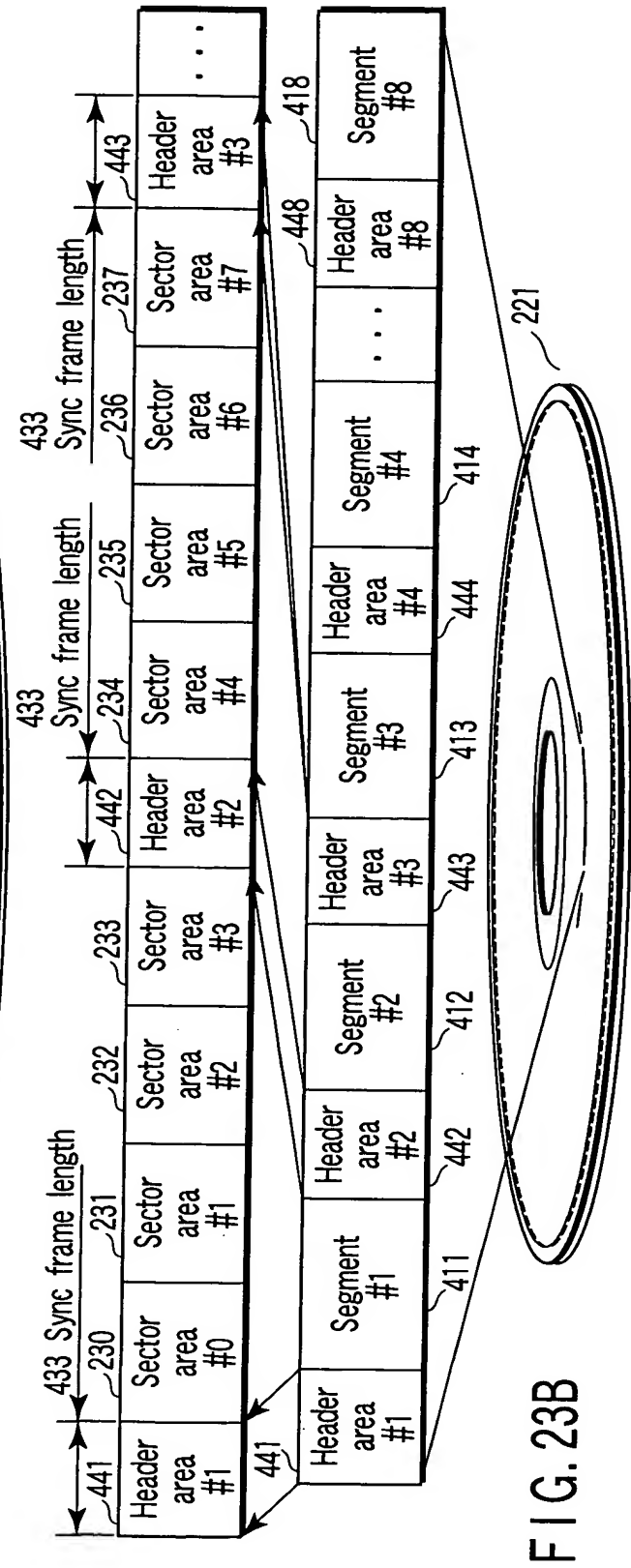
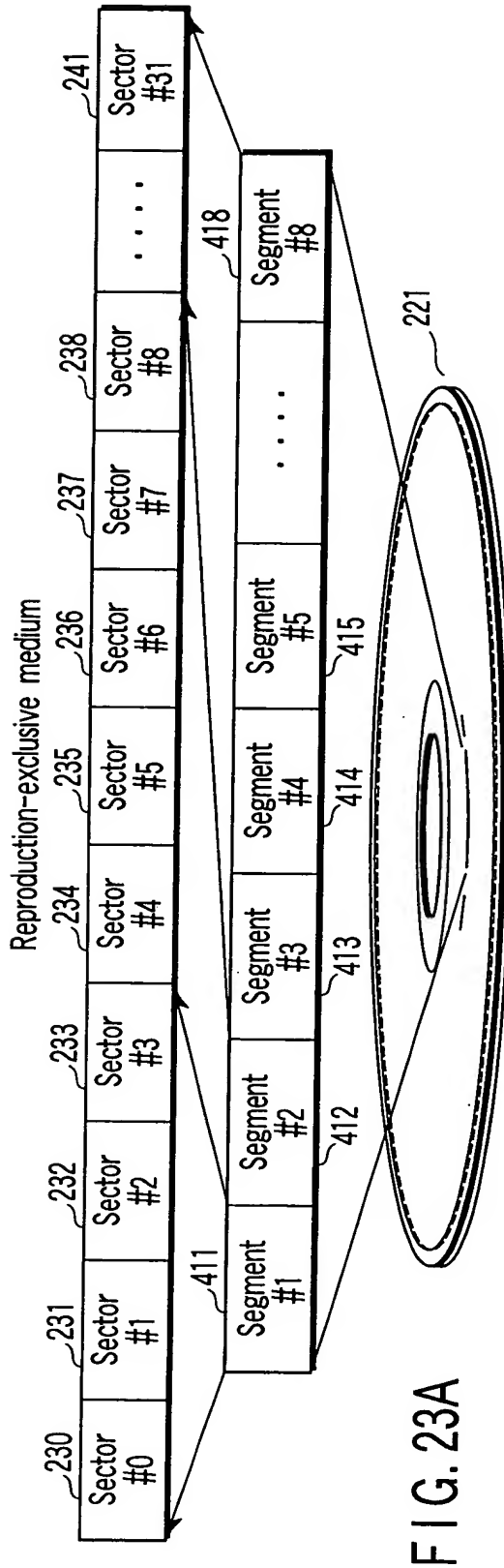


FIG. 22



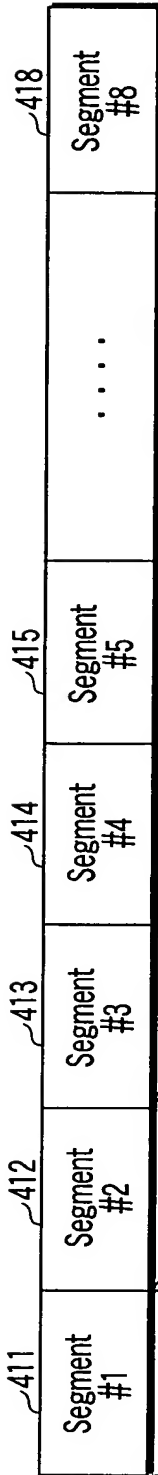


FIG. 24A

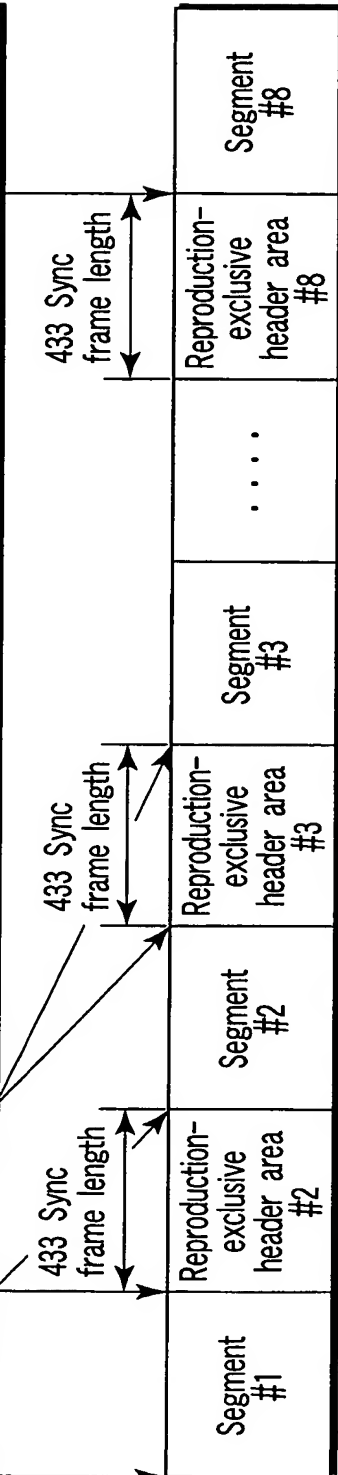


FIG. 24B

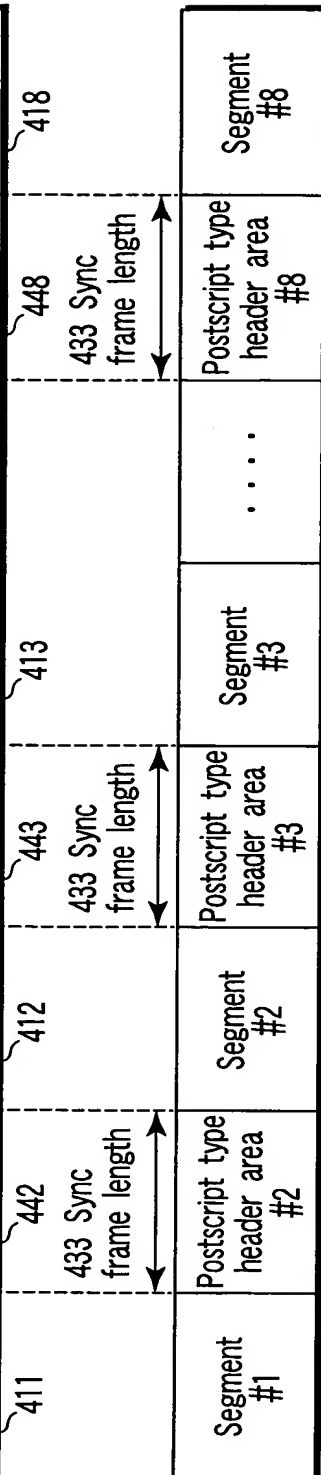


FIG. 24C

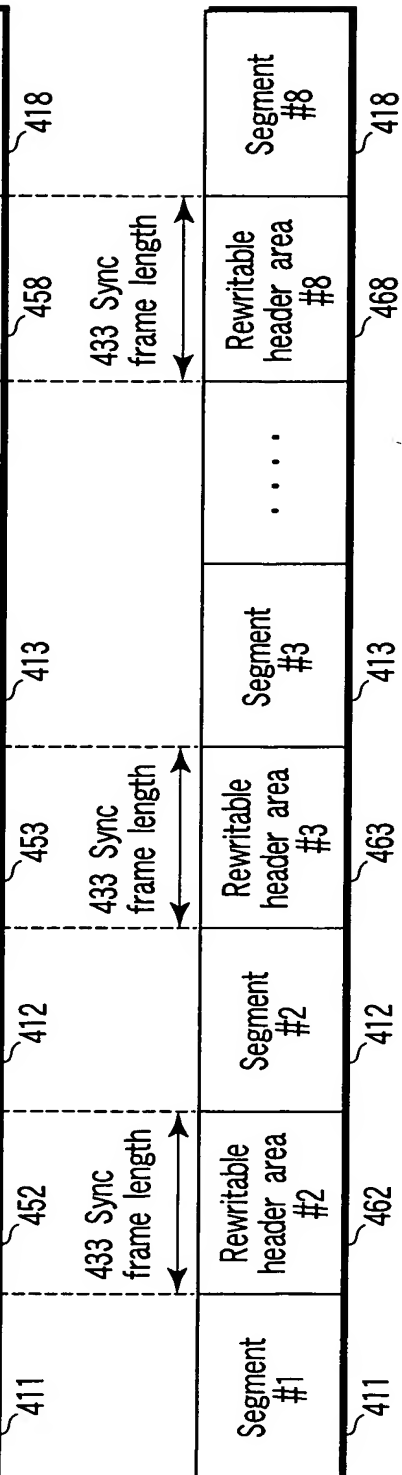


FIG. 24D

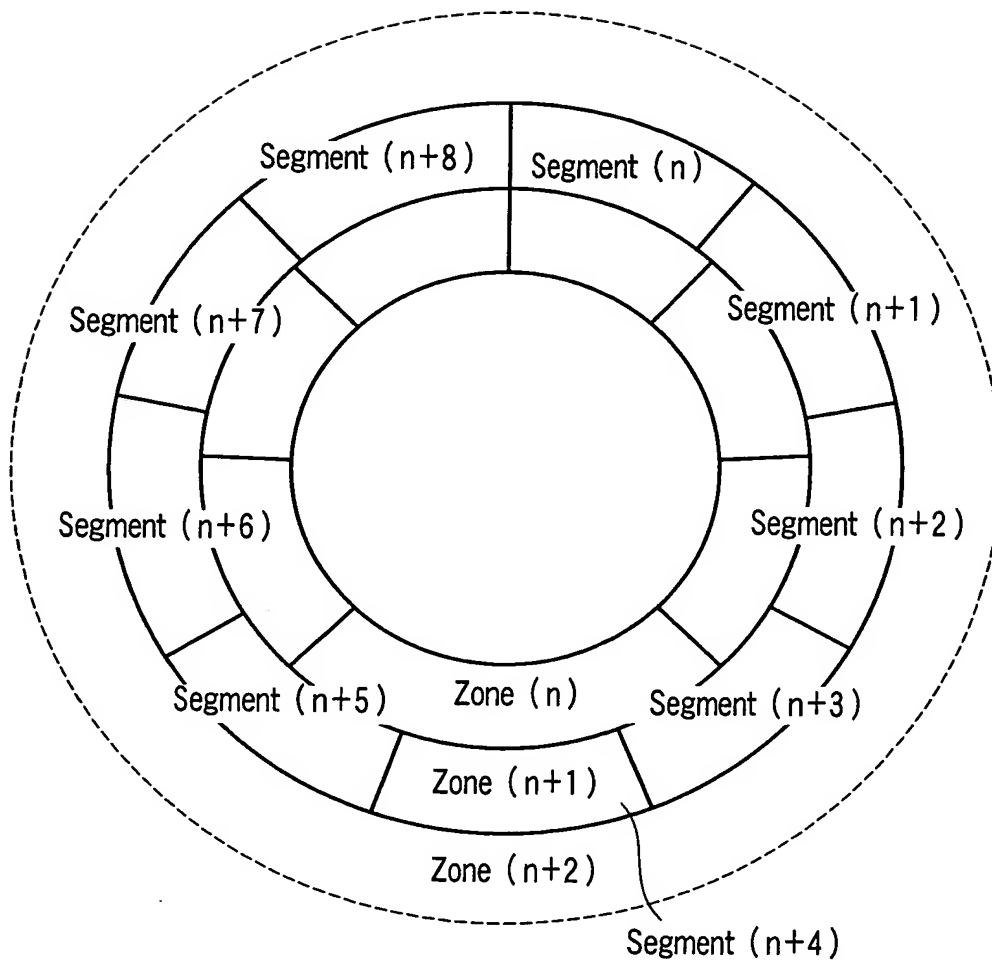
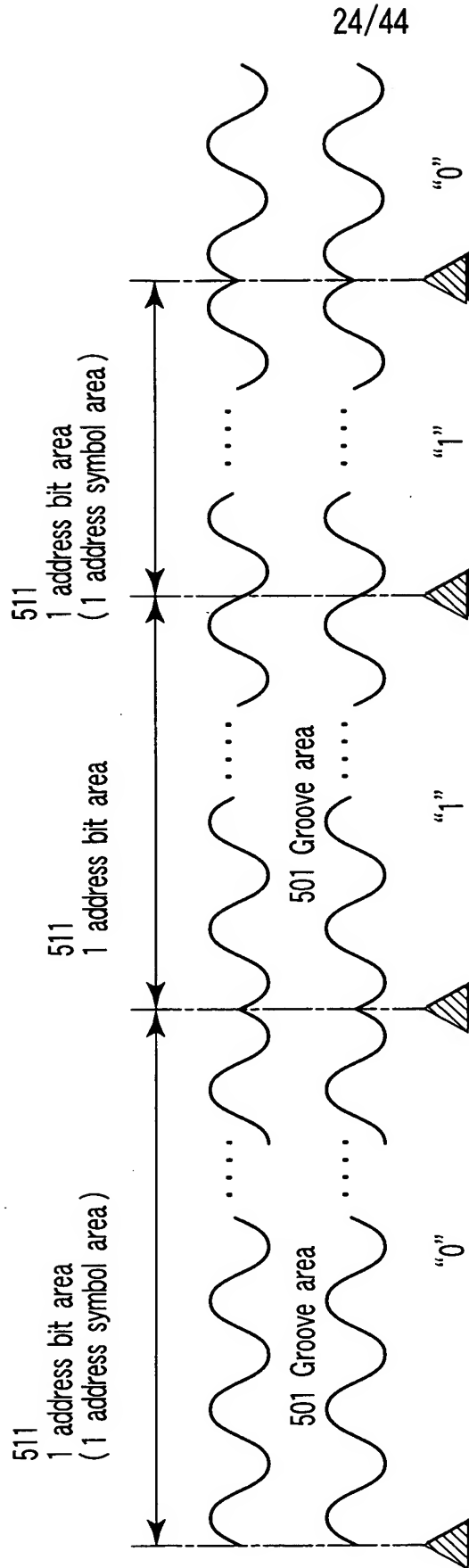


FIG. 25



- ☆ 1 address bit area 511 (expressed by 8 or 12 wobbles)
- ☆ Frequency, amplitude, and phase of wobble in 1 address bit area are fixed everywhere
- ☆ Boundary of 1 address bit area 511 (phase is shifted by 180° or 0°)

FIG. 26

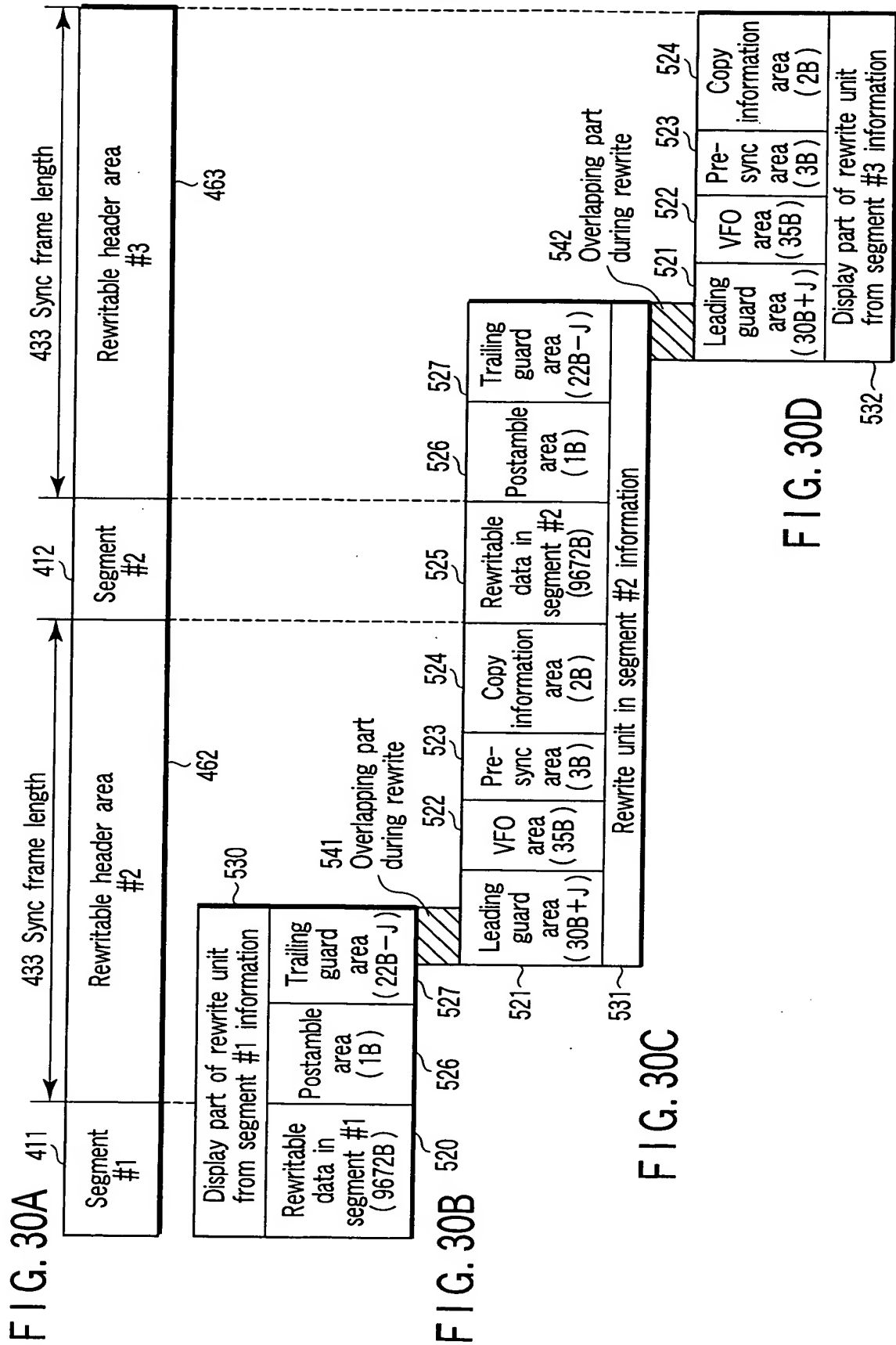
Decimal number	Conventional binary notation	Gray code notation
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

FIG. 28

Decimal number	Conventional binary notation	Special track code	Decimal number	Conventional binary notation	Special track code
0	00000	00 ... 00000	1	00001	10 ... 00000
2	00010	00 ... 00001	3	00011	10 ... 00001
4	00100	00 ... 00011	5	00101	10 ... 00011
6	00110	00 ... 00010	7	00111	10 ... 00010
8	01000	00 ... 00110	9	01001	10 ... 00110
10	01010	00 ... 00111	11	01011	10 ... 00111
12	01100	00 ... 00101	13	01101	10 ... 00101
14	01110	00 ... 00100	15	01111	10 ... 00100
16	10000	00 ... 01100	17	10001	10 ... 01100
18	10010	00 ... 01101	19	10011	10 ... 01101
20	10100	00 ... 01111	21	10101	10 ... 01111
22	10110	00 ... 01110	23	10111	10 ... 01110
24	11000	00 ... 01010	25	11001	10 ... 01010
26	11010	00 ... 01011	27	11011	10 ... 01011
28	11100	00 ... 01001	29	11101	10 ... 01001
30	11110	00 ... 01000	31	11111	10 ... 01000

FIG. 29

Note] "2n" and "2n+1" differ only in most significant bit. All other lower bits are the same.



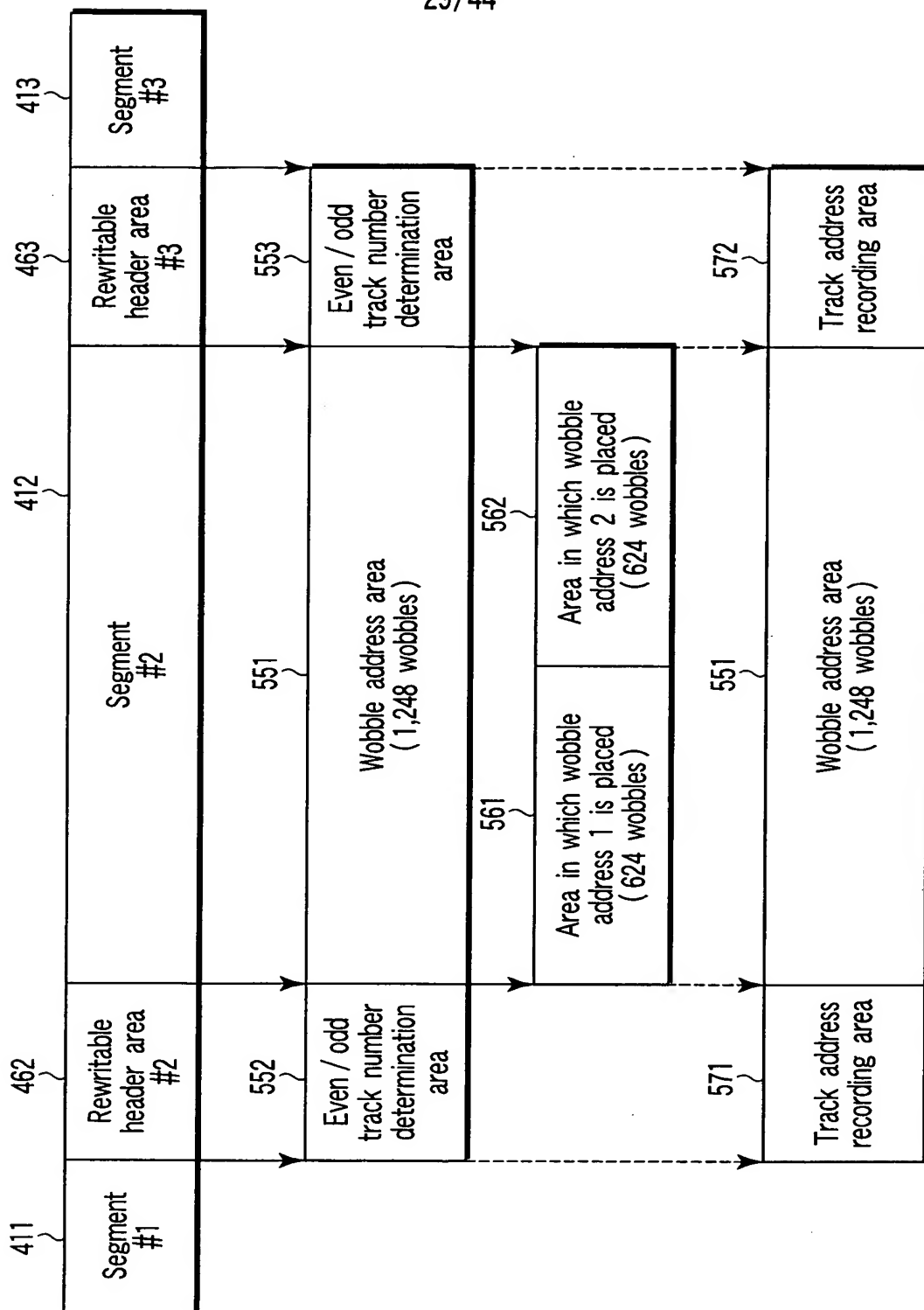


FIG. 31A

FIG. 31B

FIG. 31C

FIG. 31D

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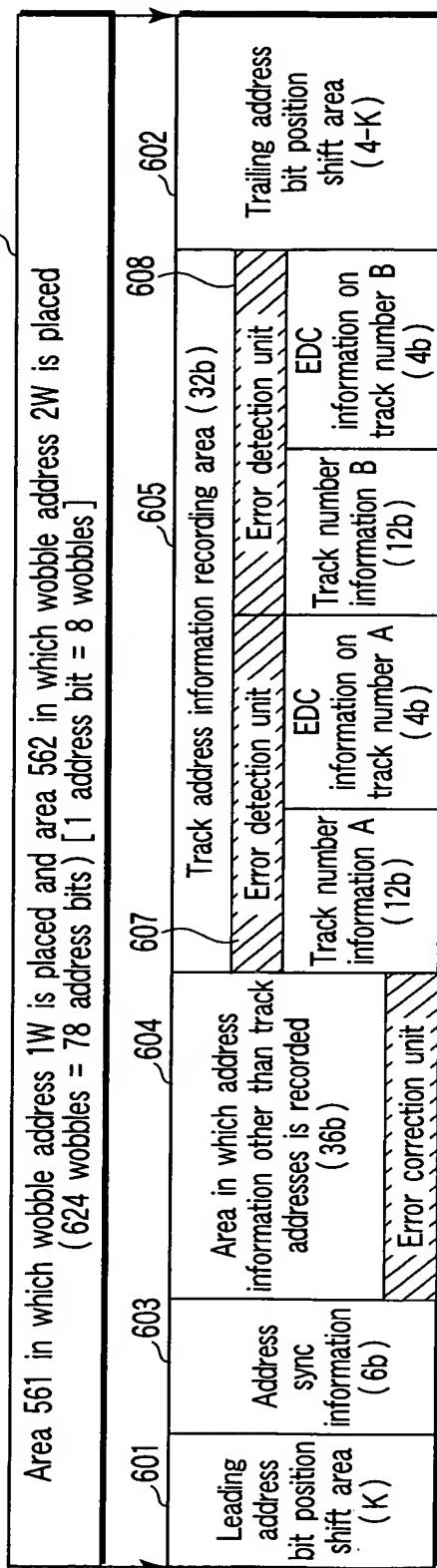


FIG. 32A

FIG. 32B

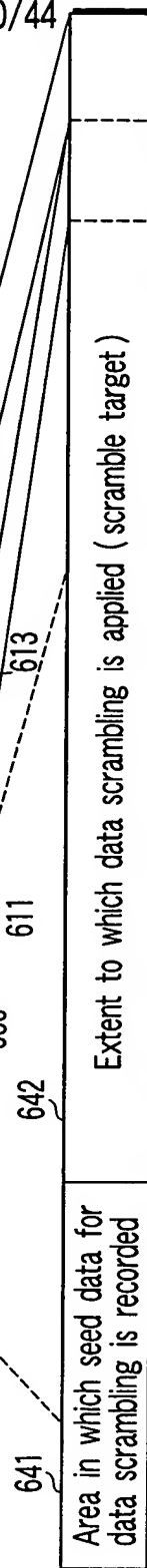


FIG. 32C

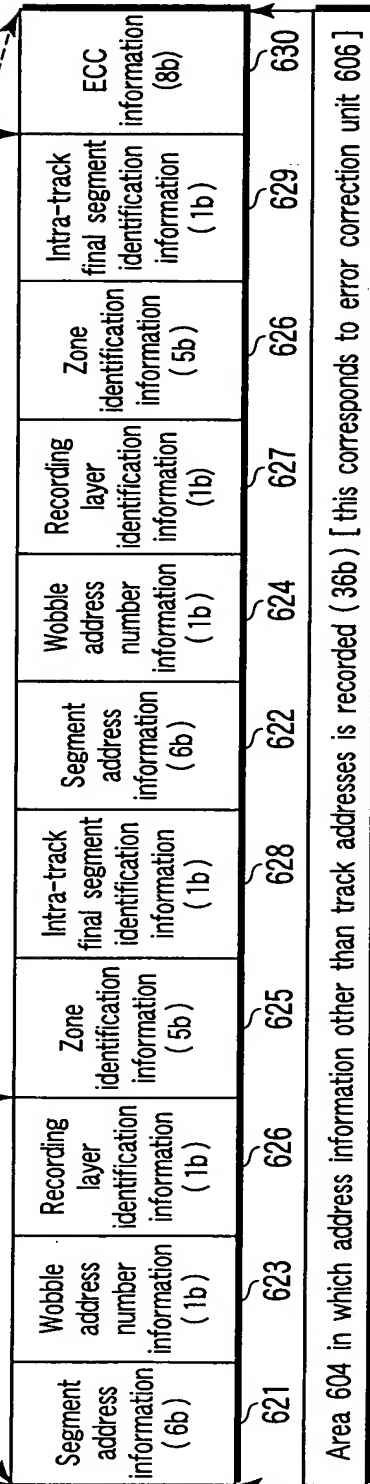
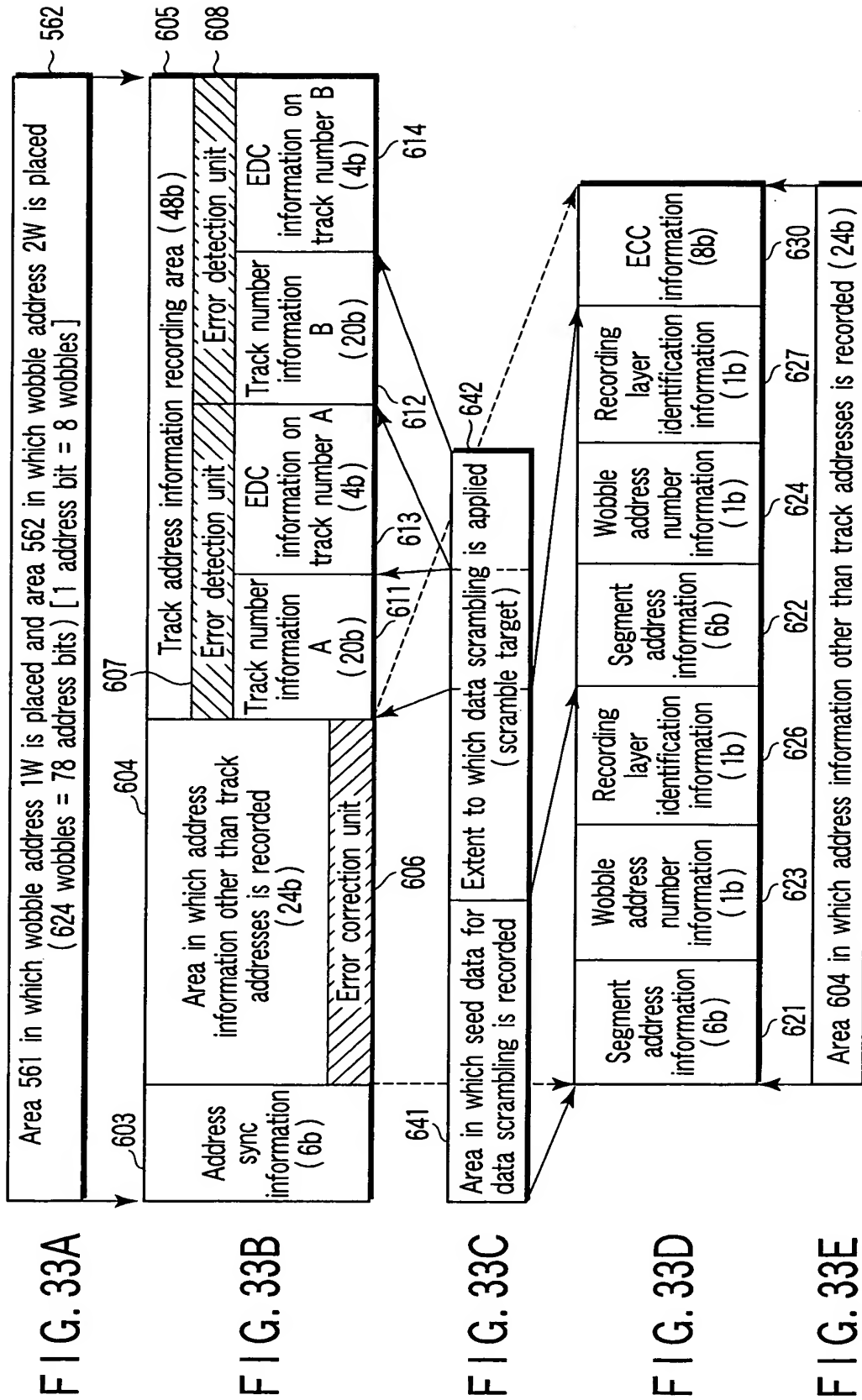


FIG. 32D

FIG. 32E



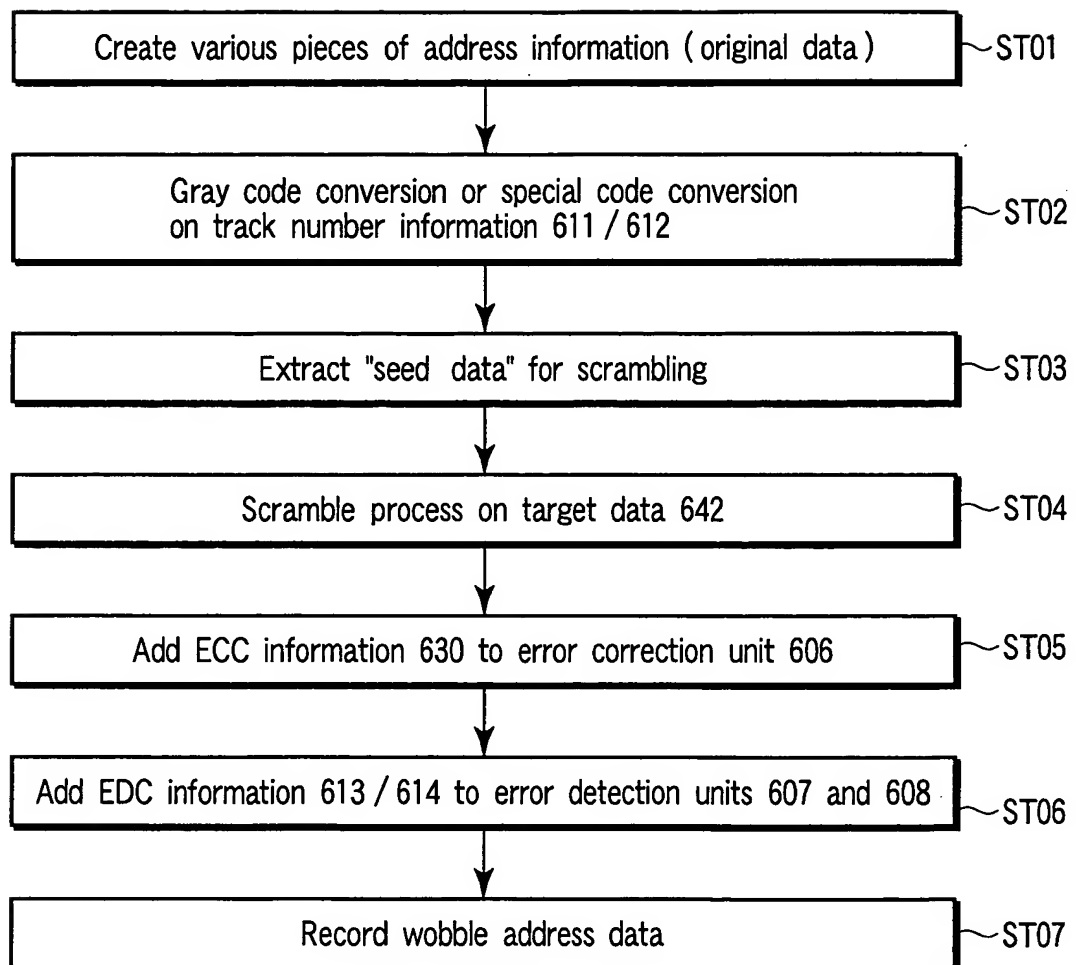


FIG. 34

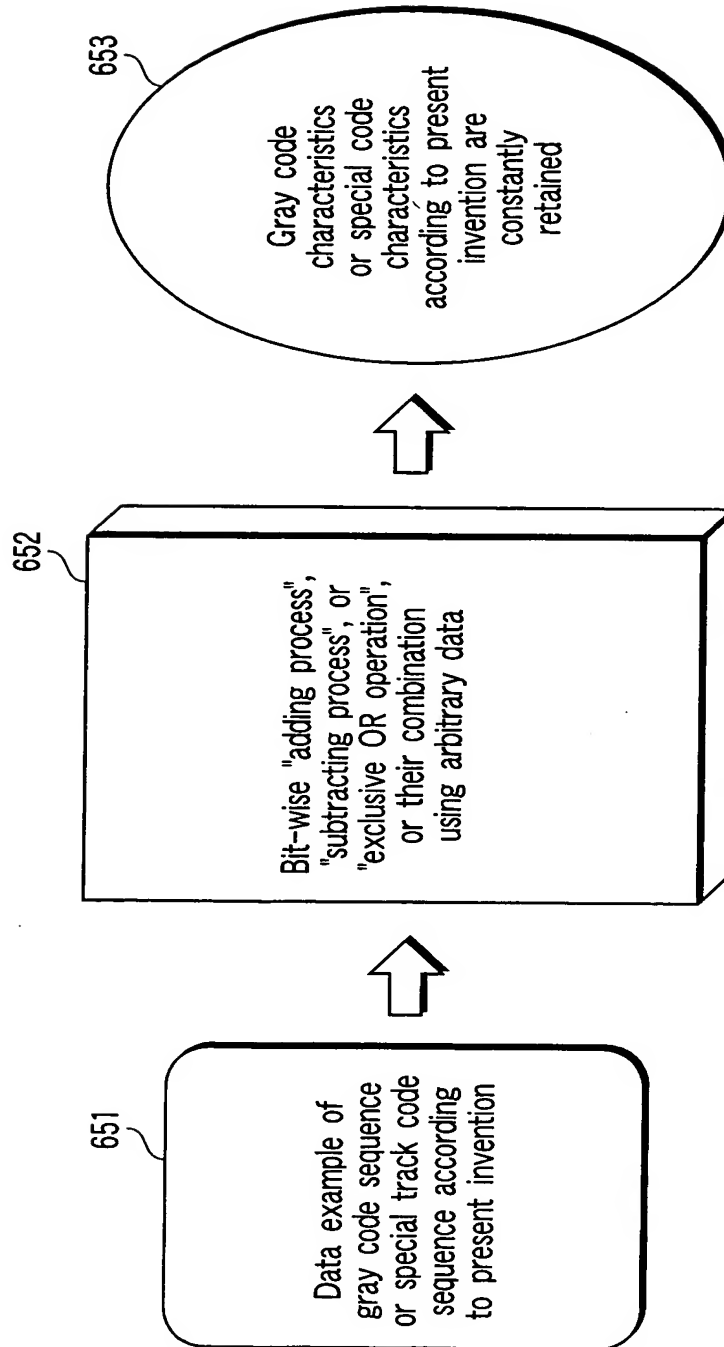


FIG. 35

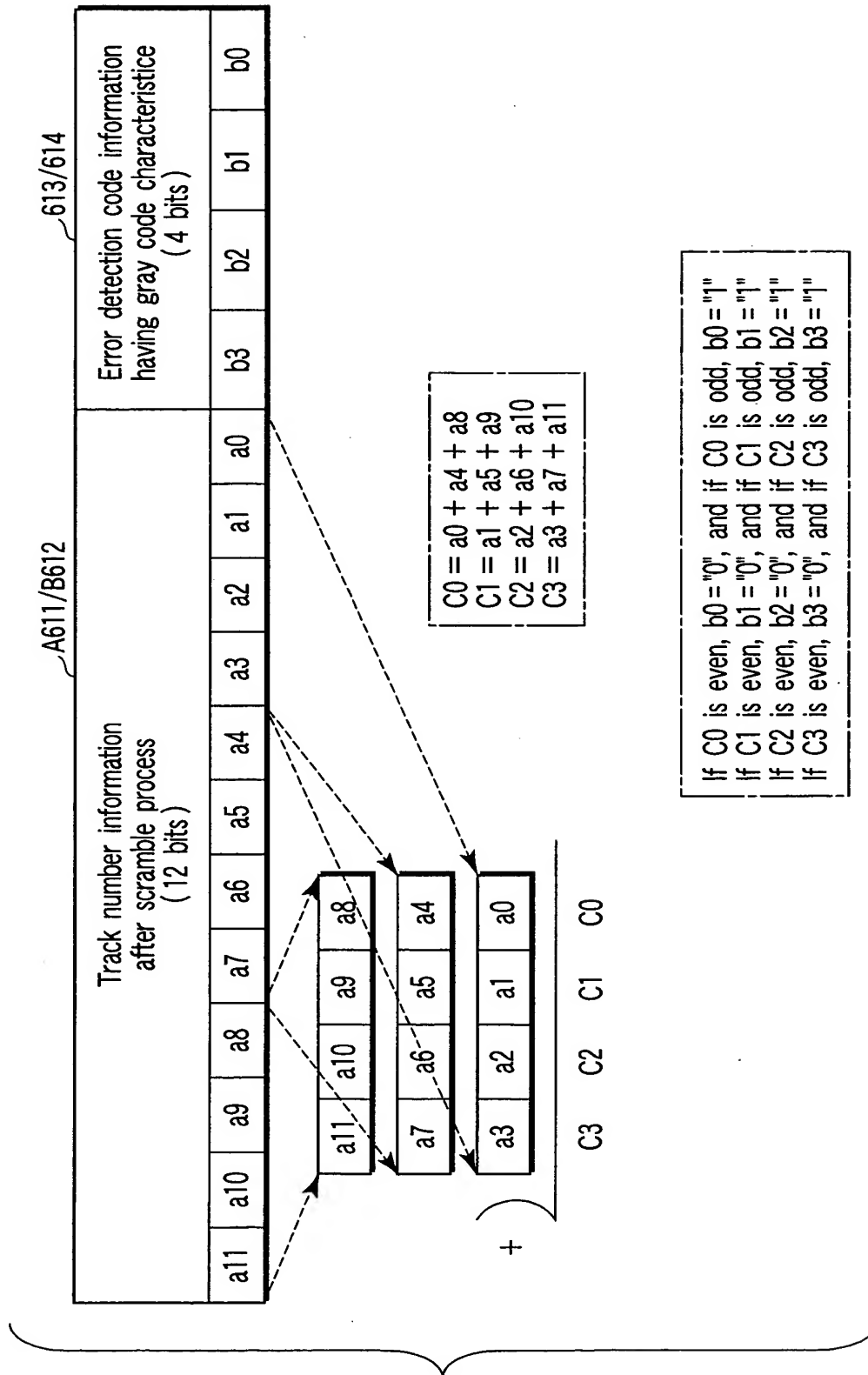


FIG. 36

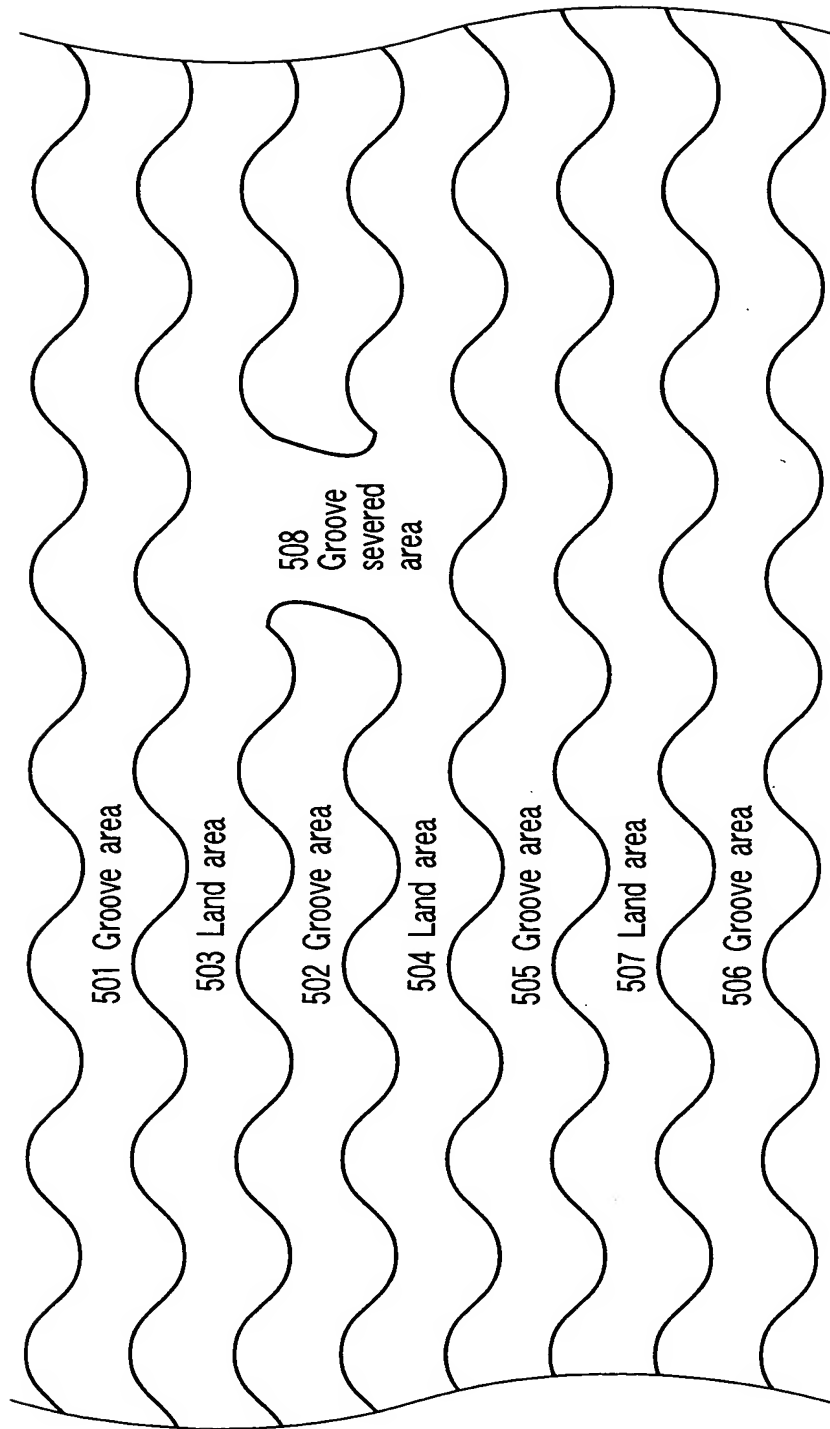


FIG. 37

L / G identification	Track number	Track number information A611	Track number information B612
Groove	$2n+3$	$2n+4$	$2n+3$
Land	$2n+3$	Indefinite ($2n+2$ or $2n+3$)	$2n+3$
Groove	$2n+2$	$2n+2$	$2n+3$
Land	$2n+2$	$2n+2$	Indefinite ($2n+1$ or $2n+3$)
Groove	$2n+1$	$2n+2$	$2n+1$
Land	$2n+1$	Indefinite ($2n$ or $2n+2$)	$2n+1$
Groove	$2n$	$2n$	$2n+1$

FIG. 38

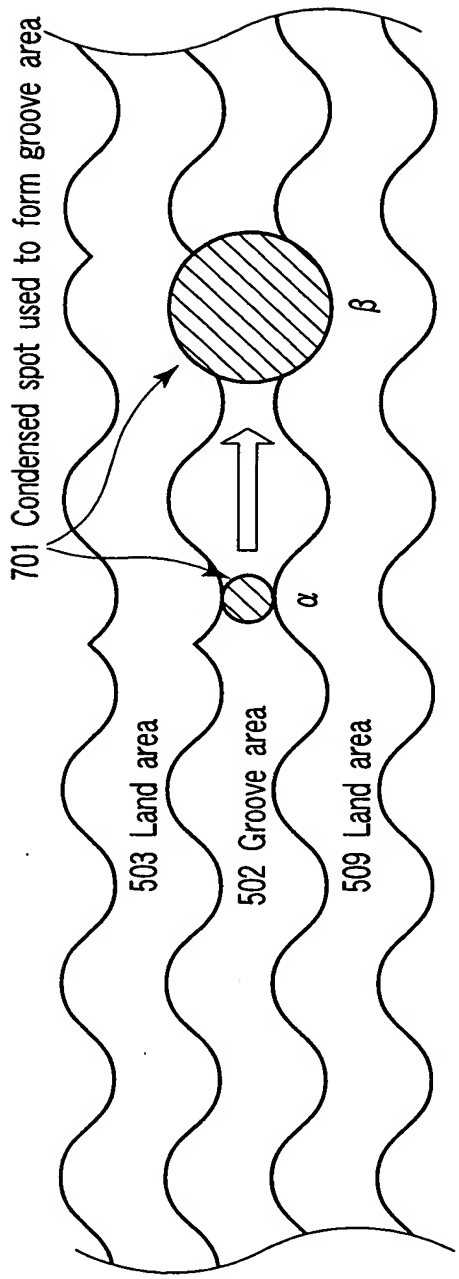


FIG. 39A

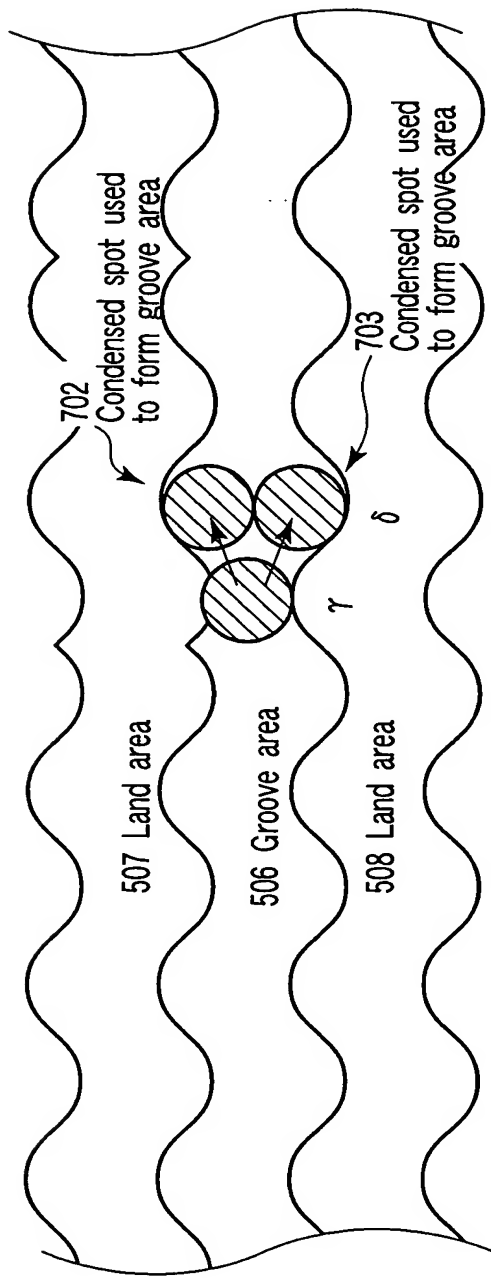


FIG. 39B

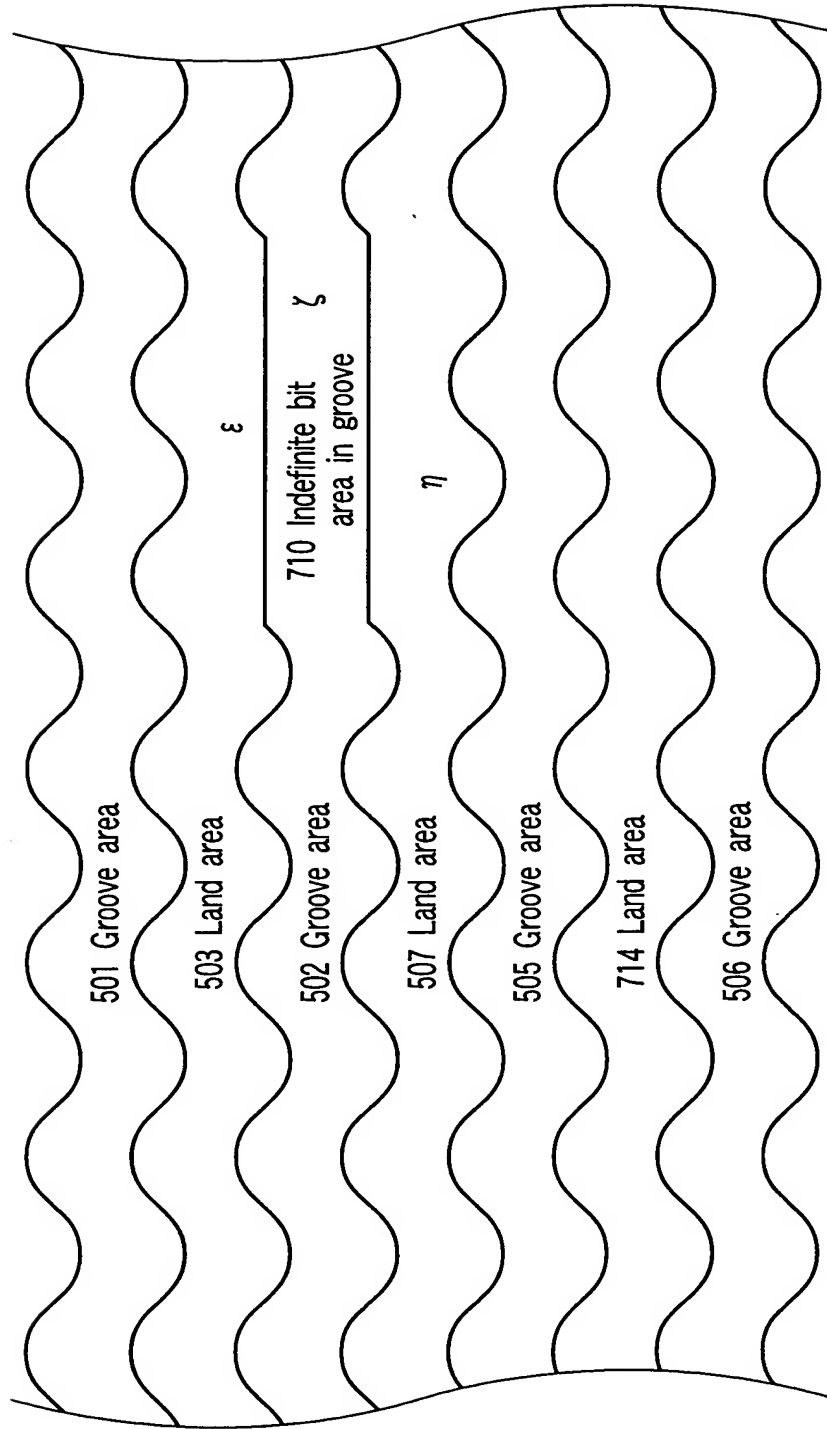


FIG. 40

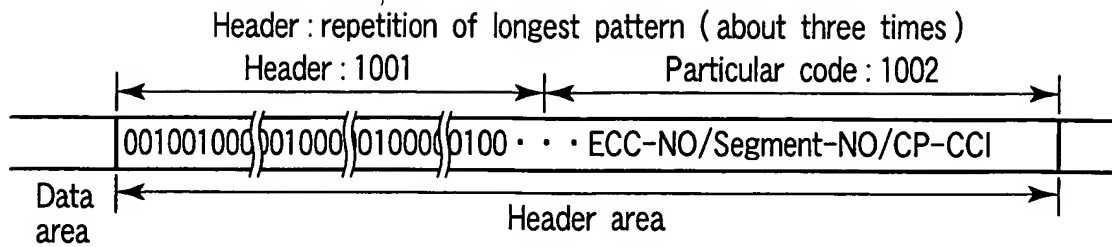


FIG. 41

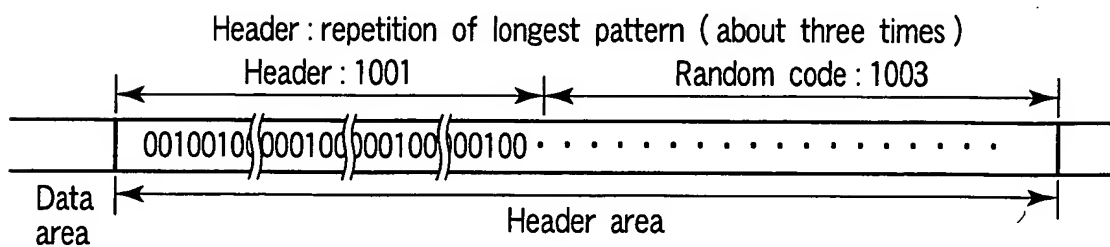


FIG. 42

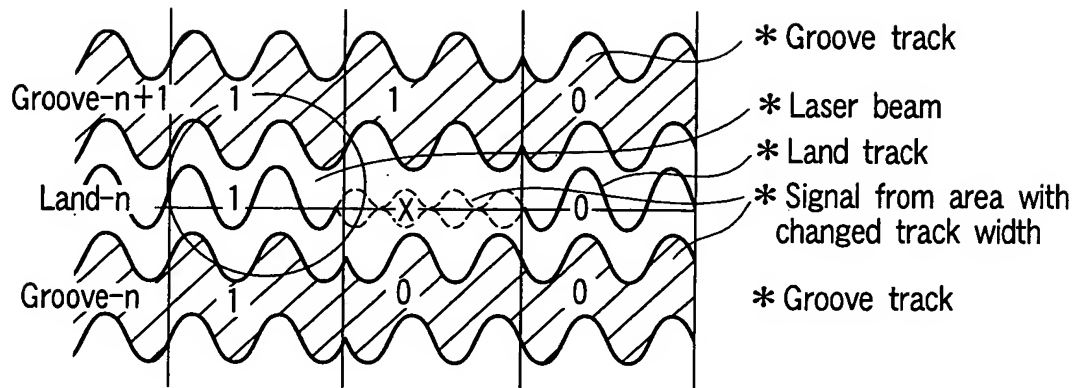


FIG. 43

Track form	Detected track number
Groove	$n+3$
Even-land ($n+2$)	$(n+2)$ or $(n+3)$
Groove	$n+2$
Odd-land ($n+1$)	$(n+1)$ or $(n+2)$
Groove	$n+1$
Even-land (n)	(n) or $(n+1)$
Groove	n

FIG. 44

G / L track	Track number	Track number determination criteria
Groove : G (n+2)	1101	
Odd-land : L (n+1)	110 *	Only 1101 or 1100 for odd-lands
Groove : G (n+1)	1100	
Even-land : L (n)	* 100	Only 1100 or 0100 for even-lands
Groove : G (n)	0100	

FIG. 45

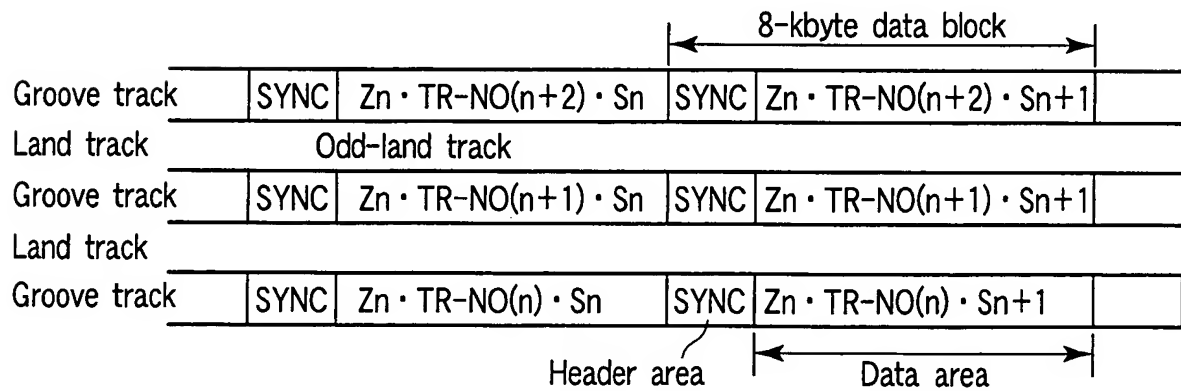


FIG. 46

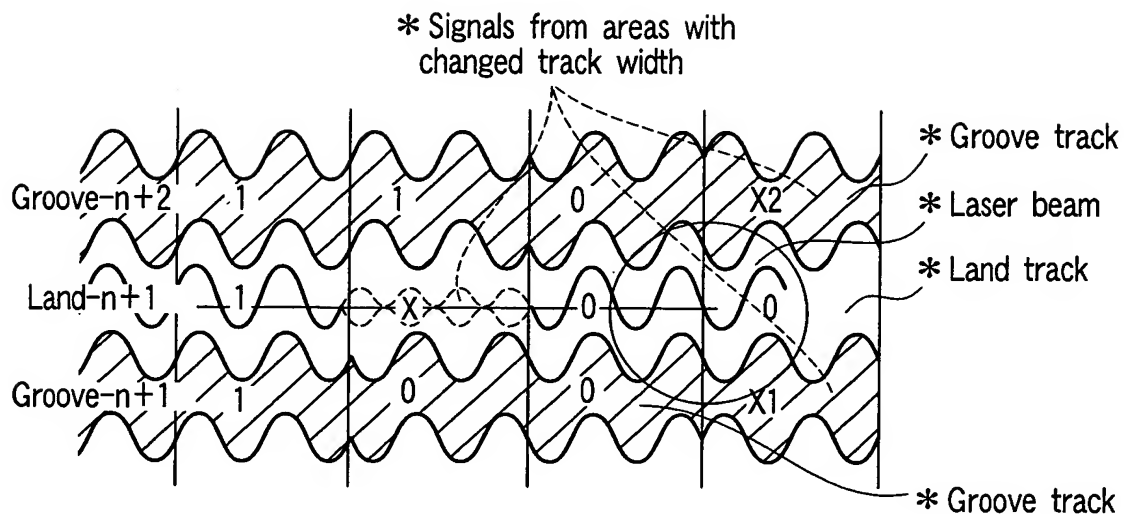


FIG. 47

Groove track	G-S 1101	L-S 11X1	G-S 1101	L-S 11X1	
Land track		L-S 1101		L-S 1100	
Groove track	G-S 1100	L-S X100	G-S 1100	L-S X100	
Land track		L-S 0101		L-S 0100	
Groove track	G-S 0101	L-S 010X	G-S 0100	L-S 010X	

FIG. 48

G / L track	Track number	Track number determination criteria
Groove : $G(n+2)$	1101X	For grooves, only leading 4 bits are effective
Odd-land : $L(n+1)$	110X0	Only 11010 or 11000 for odd-lands
Groove : $G(n+1)$	1100X	For grooves, only leading 4 bits are effective
Even-land : $L(n)$	X1001	Only 11001 or 01001 for even-lands
Groove : $G(n)$	0100X	For grooves, only leading 4 bits are effective

FIG. 49

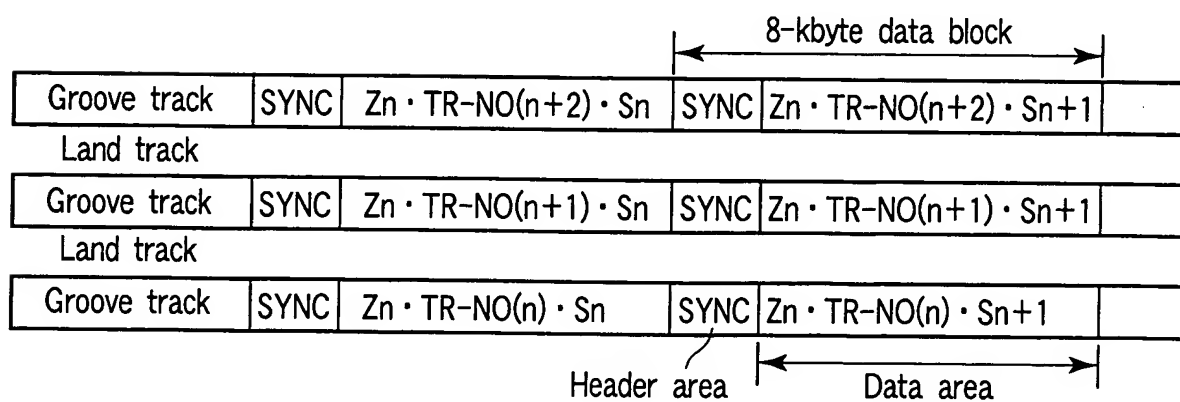


FIG. 50

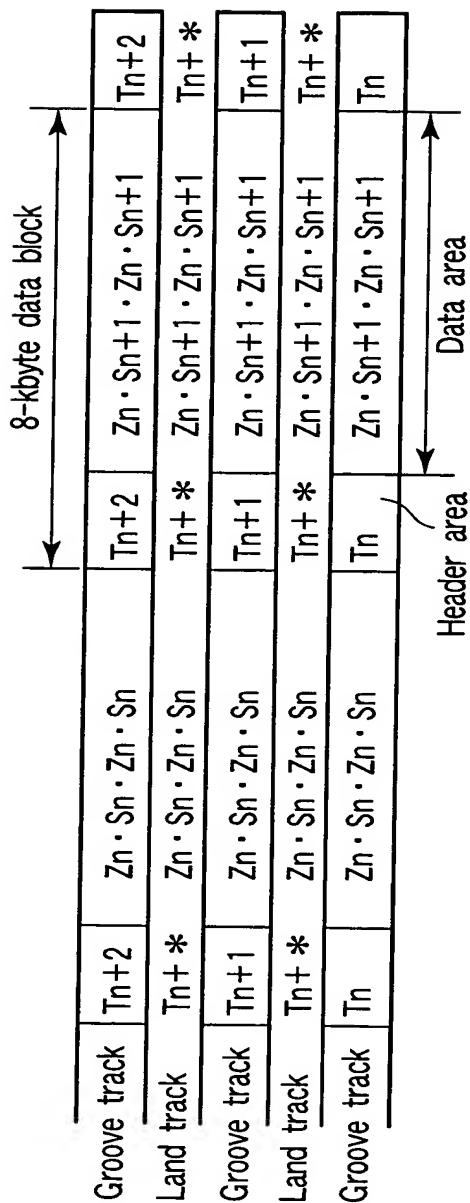


FIG. 51